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ELECTRONIC COMPUTING CIRCUITS OF THE ENIAC

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Electronic Computing Circuits of the ENIAC*

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Summary—The ENIAC (Electronic Numerical Integrator and Computer), the first electronic computing machine to be built, is a very large device (containing 18,000 vacuum tubes) compounded out of a few basic types of computing circuits. The design principles that were followed in order to insure reliable operation of the electronic computer are presented, and the basic types of computing circuits are analyzed.

Most of the design work on component circuits was devoted to constructing reliable memory circuits (flip-flops) and adding circuits (counters). These are treated in detail.

The ENIAC performs the operations of addition, subtraction, multiplication, division, square-rooting, and the looking up of function values automatically. The units which perform these operations, the units which take numerical data into and out of the machine, and those which control the over-all operation are described.

The technique of combining the basic electronic circuits to perform these functions is illustrated by three typical computing circuits: the addition circuit, a programming circuit, and the multiplication circuit.

I. INTRODUCTION

THE ENIAC (Electronic Numerical Integrator and Computer) is the first general-purpose computing machine in which the computation is done entirely electronically. It is the purpose of this paper to discuss the design of the various circuits used and to show how they are combined to make an automatically sequenced electronic computer. As an introduction, however, it is worth while to consider the general question: What is the function of the ENIAC? That is, what kinds of problems does it solve?

Very briefly, the answer to this question is that the ENIAC can solve any problem which can be reduced to numerical computation, i.e., to a finite sequence (of reasonable length) consisting of additions, subtractions, multiplications, divisions, square-rootings, and the looking up of function values. Hence, it can differentiate, integrate, solve systems of simultaneous algebraic and transcendental equations, partial differential equations, etc. The importance of high-speed electronic computation derives from the fact that there are many problems that the mathematical physicist can easily formulate but which can be solved only with great labor. The differential equations of exterior ballistics will serve as a good example of this, especially since the ENIAC was designed primarily to solve total differential equations of about this order of complexity.

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It is well known¹ that the path of a projectile in motion is described by

$$y'' = -Ey' - g$$

$$x'' = -Ex'$$

where

$$E = \frac{e^{-hv}G(v)}{C}, \quad (v = \sqrt{(x')^2 + (y')^2}),$$

g and h are fixed constants, C is a constant for a given shell, and $G(v)$, the ballistic drag function, expresses the resistance of the air to the shell as a function of its velocity. The equations are thus easy to state, but since the drag function has no simple mathematical formulation (it is actually obtained from experimental measurements, i.e., firings of shells) an analytic solution of them (that is, a solution in terms of well-known functions) is impossible. Hence, the construction of a firing or bombing table requires the numerical solution of this pair of differential equations for each set of initial conditions (muzzle velocity, angle of fire) for each type of shell, and a transformation of the results into a form suitable for use in the field or in the construction of a gun director. Each solution is called a trajectory, and the production of a firing table requires the computation of hundreds of such trajectories and a processing of the results. A skilled computer with a desk machine can compute a 60-second trajectory in about twenty hours; a differential analyzer can produce the same results in about fifteen minutes; the ENIAC can do it in thirty seconds, that is, it can compute the trajectory of a shell faster than the shell itself flies! Moreover, the ENIAC, which can handle either ten- or twenty-digit numbers, is much more accurate than a differential analyzer, and is, in fact, 1000 times as fast as any machine which gives comparable accuracy.

II. GENERAL CIRCUIT-DESIGN CONSIDERATIONS

War circumstances made it imperative to construct the ENIAC out of conventional electronic circuits and elements with a minimum of redesign. This fact, together with the ordnance requirements for capacity, speed, and accuracy, led to an extremely large electronic machine. The ENIAC contains about 18,000 tubes,² 70,000 resistors, 10,000 capacitors, 6,000 switches, etc. It is 100 feet long, 10 feet high, and about 3 feet deep. The filaments require 80 kilowatts of power, the direct-current power supplies produce 40 kilowatts, and the blower system consumes 20 kilowatts of power.

It is clear that, if an electronic device with 18,000 tubes in it is to be successful, the component circuits must be extremely reliable. This is especially true of a

¹ G. A. Bliss, "Mathematics for Exterior Ballistics," John Wiley and Sons, New York, N. Y., 1944, chap. 2.

² Actually 18,000 envelopes, many of them containing two triodes.

and for programming the various operations to be performed. These control circuits are compounded out of three very simple types of circuits: the electronic representations of the logical concepts of "and," "or," and "not." The "and" operation is performed by a "gating" or "switching" tube; for example, a pentagrid tube with the first and third grids used as the control elements (such as tube 9 of Fig. 3). A gate tube draws current only when both grids are brought to cathode potential, and hence one grid switches a signal applied to the other grid into and out of the plate circuit. Such a tube is symbolized in the block diagrams of Figs. 2 and 4 by a square with two inputs and one output (e.g., tube 2 of Fig. 2). Gating can also be done by means of a circuit which is the dual of this; a number of tubes connected to

the following tube is not sensitive to differences in amplitude.) The dual of this circuit consists of a two-input tube (such as a pentagrid tube) which is kept on normally, so that a negative signal to either input will be transmitted to the output without affecting the other input. The "not" operation is, of course, performed by an inverter tube (such as tube 3 of Fig. 2 and tube 6 of Fig. 3). In all the figures, normally conducting tubes are shaded and normally nonconducting tubes are left unshaded.

IV. FLIP-FLOP AND COUNTER DESIGN

The flip-flop circuit used in the ENIAC is shown in Fig. 3 (tubes 1, 2, 3, and 4). In the design of such a circuit two aspects need to be considered: (1) the steady-state stability, depending upon the direct-current connections, and (2) the flipping or triggering action, depending upon the alternating-current connections as well. These will be discussed in turn.

(1) A flip-flop has two stable states because of the direct-current connections from the plate of each tube to the grid of the opposite tube (R_2 , R_5 of Fig. 3) which cause the conducting tube to bias the nonconducting tube negatively, and the nonconducting tube to bias the conducting tube positively. The resistors R_2 and R_3 (similarly R_5 and R_6) form a direct-current voltage step-down circuit changing the direct-current level of the plate signal to the proper direct-current level for the grid, and must be selected so that the biases are correct. The difference between the voltage at the plate of tube 3 when it is conducting and nonconducting depends upon the sizes of R_1 , R_2 , and R_3 , relative to the plate resistance of tube 3 (similarly for tube 4), and the amount of this signal that is applied to the grid of tube 4 depends on the ratio R_2/R_3 . In designing the circuit the expected variations in resistor values and plate resistances of the tubes, and also the power-supply regulation, must be considered and the parameters selected so that the stability of the circuit will not be greatly affected by these variations. The stability needed in the ENIAC was attained by making these resistors roughly equal ($R_1 = R_4 = 39,000$ ohms and $R_2 = R_3 = R_5 = R_6 = 47,000$ ohms) and about six to eight times as large as the plate resistance of an average 6SN7 tube (as measured when the grid of the tube is driven positive).

(2) The design of the circuit from the point of view of dynamic operation leads to a compromise between two opposing factors; the actual flipping of the circuit and the recovery of the circuit so that it will be ready for re-setting. Increasing the values of R_1 , R_2 , and R_3 will increase the gain of the circuit and hence accelerate the flipping action; and increasing the value of C_1 will decrease the alternating-current impedance from plate to grid and hence will accelerate the transfer of the plate signal to the grid. But large values of R_1 , R_2 , R_3 , and C_1 will delay the return to the quiescent state (ready for the next operation) by making the time constant of the circuit large. The actual value chosen for C_1 (and C_2) was

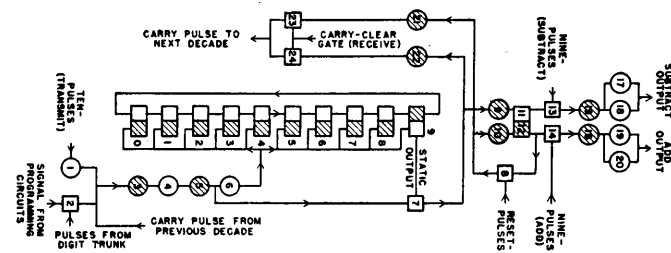


Fig. 2—Block diagram of accumulator decade circuit.

a common load resistor and so arranged that any one tube when conducting draws sufficient current to keep the following tube cut off is a representation of the concept "and," for only if *all* of these tubes are cut off will the following tube be operated.⁷

The "or" operation is performed by a "buffing" circuit. Such a circuit may consist of two or more normally nonconducting tubes with a common load resistor in either the plate circuit (see tube 8 of Fig. 3) or the cathode circuit (see tube 7 of Fig. 3). A positive input signal

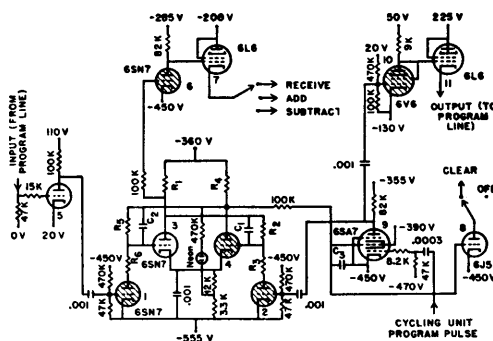


Fig. 3—Accumulator program control circuit (simplified).

to any of these tubes will be transmitted to the output without affecting the inputs of the other tubes. (If more than one tube is made conducting, the output signal is increased, but this has no effect on the computing since

⁷ W. B. Lewis, "Electrical Counting," Cambridge University Press, Cambridge, England, 1942, p. 61.

25 micromicrofarads. In all cases where a flip-flop was used by itself (i.e., not in connection with other flip-flops as in the counter of Fig. 1), the flipping tubes 1 and 2 were built into it in order to speed up the action by amplifying the triggering pulse and by avoiding the additional capacitance of a long lead going into the grid circuit. The flip-flop shown in Fig. 3 can be set in about one microsecond and is ready to reset in about four microseconds; in the ENIAC it always has at least 2.5 microseconds in which to be set, and is never reset sooner than ten microseconds after being set.

The design of a vacuum-tube counter can be based on the flip-flop in either of two ways: (1) A counter can be made by using a flip-flop for each stage as in the circuit of Fig. 1.⁸ Since a flip-flop is required for each stage, this type of counter is known as a two-tubes-per-stage counter. (2) A counter with only one tube per stage can be made by generalizing the flip-flop so that it has as many stable states as tubes.⁹⁻¹² In such a counter the static connections consist of resistors going from the plate of *each* tube to the grid of *every* other tube. This means that (in contradistinction to the two-tubes-per-stage counter) this type of counter becomes inherently more complicated as the number of stages increases. For this reason the other type was adopted for the decade counters (used for registering and storing decimal digits). For a binary counter (needed for storing the signs of numbers) the one-tube-per-stage type (Fig. 5) proved superior.

The action of the circuit of Fig. 1 may be explained with reference to the block diagram of Fig. 2. The counter of Fig. 2 registers the digit 9, since the last flip-flop has been triggered (similarly, Fig. 1 registers the digit 0). The triggered flip-flop is the only one to respond to an incoming positive pulse which is applied to all flip-flops; as it is reset it gives out a positive pulse which triggers the next stage. In this manner the counter advances one stage on receiving a pulse, and hence is an adder as well as a register. It may be cleared to zero by applying a negative pulse to the input of the 6Y6 clearing tube. Clear leads go from this tube and from the balancing 1200-ohm resistor to each stage, the connections to the zero stage being reversed so that this stage is left in a triggered state.

There are the following five basic considerations or principles which enter into the design of a counter circuit: (1) The first of these has to do with the prevention of oscillation. As Fig. 2 shows, in a ring counter there are a number of tubes connected from plate to grid re-

peatedly, making a closed loop. Consequently, if at any time all of the tubes in this loop are conducting, the circuit may oscillate. Though possible oscillation may be prevented by adjusting the circuit parameters so as to reduce the over-all gain per stage, such a solution slows

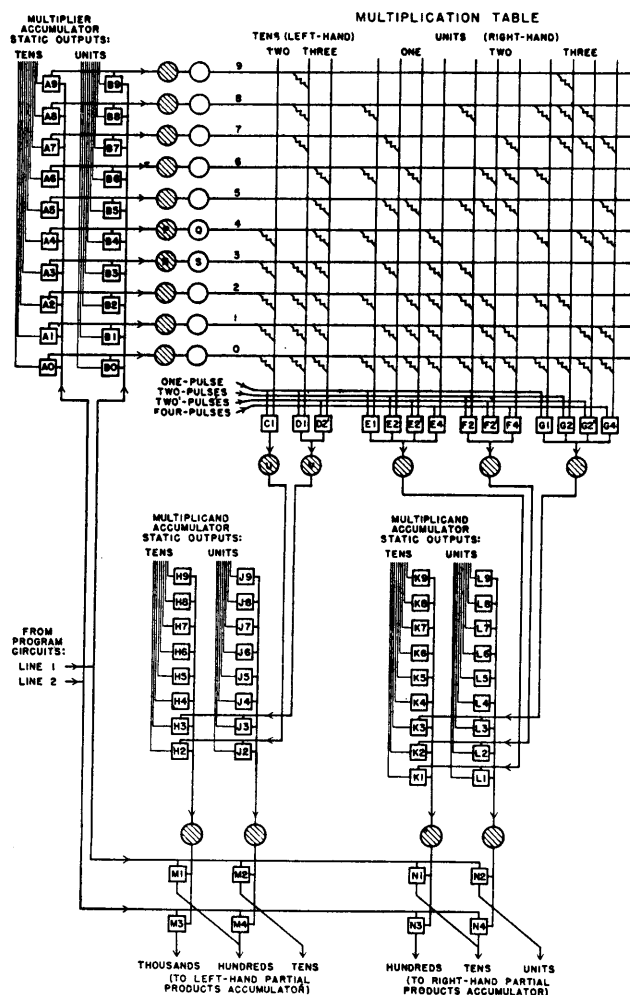


Fig. 4—Block diagram of multiplication circuits.

up the operation of the counter. For this reason counter configurations, in which the pulsing action would establish such an oscillatory loop, were rejected in the ENIAC.

(2) There are a large number of interconnections in a counter. In addition to the internal connections of each flip-flop stage, there are coupling connections between stages, connections to the common pulse bar, connections for clearing the counter to the zero position, and static output connections for operating indicating neon lamps and associated vacuum tubes. It is desirable to arrange the circuit so that there are a minimum of connections going to any one element of the tube. Hence it is disadvantageous to pulse the tubes on the grids, since these elements are already used for the internal connections of the flip-flop and for coupling connections between stages. The decade counter of Fig. 1 is pulsed on the cathode, while the binary counter of Fig. 5 is pulsed on the plate.

⁸ This circuit is a modification of one suggested to us by RCA Laboratories, Princeton, N. J.

⁹ See page 91 of footnote reference 6 for a five-stage one-tube-per-stage counter. The binary (scale-of-two) counter of Fig. 5 is the simplest case of a one-tube-per-stage counter.

¹⁰ E. C. Stevenson and I. A. Getting, "A vacuum-tube circuit for scaling down counting rates," *Rev. Sci. Instr.*, vol. 8, pp. 414-416; November, 1937.

¹¹ H. Alfven, "A simple scale-of-two counter," *Proc. Phys. Soc.*, vol. 50, pp. 358-359; May, 1938.

¹² H. Lifschutz, "A complete Geiger-Müller counting system," *Rev. Sci. Instr.*, vol. 10, pp. 21-26; January, 1939.

(3) A cathode-pulsed decade counter has another advantage over one pulsed on the grid, e.g., it has no undesirable modes of operation. For a counter to operate correctly, only one flip-flop should be in the "set" position at any one time. In a counter pulsed on the grids, it is possible for several flip-flops to be in the "set" position at one time and for the counter nevertheless to count around. This is impossible in the cathode-pulsed counter

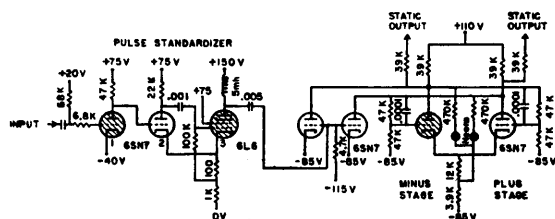


Fig. 5—Binary ring counter.

of Fig. 1, because the grid biases are obtained from the cathode resistors. If more than one stage were set, this would produce such a large negative bias that only one stage would remain set.

(4) The fourth design principle concerns the charging of grid capacitors. If a positive pulse is applied to a grid via a capacitor, the capacitor will acquire a charge. Now if the tube is conducting only while the pulse is present, the capacitor is charged through the low impedance of the (positive) grid to the cathode, but must be discharged through the relatively high bias resistor. Hence, under certain duty cycles, a charge may collect on the capacitor, changing the effective bias. The magnitude of this effect will clearly depend upon the duty cycle, and since a counter used in a computing machine has a variable duty cycle, the result would be for the effective bias to change with the conditions of operation. For this reason (and the same considerations hold true for all circuits in the ENIAC) direct rather than capacitive coupling is used with positive pulses under these circumstances.

(5) The last design principle has to do with the delicate timing involved in the operation of electronic counters. An input pulse affects only the flip-flop which is triggered; e.g., stage 9 in Fig. 2. As stage 9 is reset it produces a pulse which triggers the next flip-flop (stage 0), and if the input pulse is still present on the pulse bar, it opposes this action. A similar situation obtains in the binary counter of Fig. 5. When this counter is being flipped, there will be a point at which the currents in the two tubes are equal; at this point the previous state of the counter is not remembered in the tubes, but by means of the charges stored on the capacitors connecting the plate of one tube to the grid of the other, and the action of these charges is opposed by the input pulse. Thus the effects of the input pulse and the internal pulse going between the stages of a counter are opposed to one another, so that the counting action depends on the circuit's taking the difference between the two signals. The

counting action can be made determinate by making the time constant of the input pulse circuit shorter than the time constant between stages (and that shorter than the period between pulses, of course), and this is done in the circuits of Figs. 1 and 5. Nevertheless, the operation of the counter depends very critically upon the shape of the incoming pulse, so that the pulse-forming circuit of Fig. 5 is used with all the counters of the ENIAC.

The counters of Figs. 1 and 5 will operate over a range of frequencies from a few pulses a second to 200,000 pulses per second. To provide a safety factor of two to one they are operated in the ENIAC at a maximum rate of 100,000 pulses per second. At this speed the decade counter will operate with a direct-power supply voltage variation of from 100 to 500 volts; the circuit voltage is actually maintained at 195 ± 10 volts. Altering the resistors and capacitors of the decade circuit as much as ± 20 per cent and replacing the tubes with others having six times the plate resistance (6SL7's) only reduces this voltage range to 190 to 370 volts. At a frequency of 200,000 pulses per second the binary counter will operate with a direct-current power-supply tolerance of from 10 to nearly 1000 volts.

V. UNITS OF THE ENIAC

The ENIAC consists of thirty separate units (in addition to the power supplies and power control equipment), each containing from 500 to 1500 vacuum tubes. There are nine different types of units, each type having electronic circuits capable of performing a certain operation, and circuits which locally control the operation of the unit. The particular operations which are to be carried out and the arrangement and number of these operations are determined by the setup of a problem on the machine. The units are arranged linearly in the shape of a U, with coaxial transmission lines passing by the front of each unit. A set of eleven such lines, capable of carrying simultaneously from one unit to another the groups of pulses representing a ten-digit signed number (these pulses are called "digit pulses"), is called a "digit trunk." A single line, used to carry a "program pulse" from one unit to another, is called a "program line."

The accumulators (of which there are twenty), the high-speed multiplier, and the divider-square-rooter, are units which perform arithmetic operations. Each accumulator is capable of storing a ten-digit (decimal) signed number,¹³ of receiving such a number (in the form of pulses coming over a digit trunk) and adding it to its contents, and of transmitting (in pulse form) the number stored additively or subtractively with or without clearing¹⁴ after the transmission. The addition of two numbers requires the simultaneous operation of two accumulators: one converts the digits held in its counters into pulse form and transmits them over a digit trunk to

¹³ Provision is also made for interconnecting the accumulators and other units so that twenty-digit numbers can be handled.

¹⁴ The accumulator may be cleared to zero, or to zero in nine decades and to five in one decade, for rounding off.

the other, which receives them and adds them to its contents (see Section VI-A). An addition takes only 1/5000 second; this period of 200 microseconds is called an addition time (see Fig. 6).

It should be noted that the accumulator combines the functions of an electronic adder with those of an electronic register; it is for this reason that there are twenty of them. In addition to being used for adders they are used by the high-speed multiplier for storing the multiplier and the multiplicand, and for accumulating the partial products; by the divider-square-rooter for storing the numerator, denominator, square-root, and quotient, and for shifting remainders; by the function table for storing the argument and receiving the function value; and by the printer for storing the numbers to be punched until they are transferred to relay (electromechanical) registers.

Accumulators may be used for subtracting as well as for adding. Since the counters of the accumulators operate in one direction only (they cannot count backwards), subtraction is done by counting the counters around through zero up to the position to which the counters would have gone, had they counted backwards. This is accomplished by means of a complement system of representation. A negative number ($-x$) is represented as a complement with respect to 10^{10} ; that is, $-x$ is expressed as $(10^{10} - x)$ with a sign indication to show that it is a complement. (If twenty-digit numbers are being handled, complements are taken with respect to 10^{20} .) When an accumulator is programmed to transmit subtractively, it will transmit, not the number it holds, but the complement of the number it holds. All units of the ENIAC are capable of handling both positive numbers and complements.

The high-speed multiplier is capable of multiplying two ten-digit numbers and producing a full twenty-digit product (if needed) in 13 addition times or 2.6 milliseconds. Its operation is described in Section VI-C. The divider-square-rooter is a unit which controls the operation of certain accumulators so that they form a quotient or a square root. It does this by a process of repeated subtractions and additions, so the time required is relatively long and depends upon the numbers involved; on the average, 125 addition times, or 25 milliseconds, are required for ten-digit numbers.

Although computation with the ENIAC is done exclusively by electronic means, numerical data are supplied to the machine and the answers are taken out by electromechanical methods. While a computation is in progress, numerical data are supplied to the ENIAC by means of an International Business Machine card reader in conjunction with the constant transmitter. The card reader reads standard punched cards and gives out electrical signals which set up relays in the constant transmitter. These relays in turn operate gate tubes which emit pulses that are transmitted over the digit trunks whenever needed. The results of a computation are punched on cards by an International Business Ma-

chine card punch operating with signals received from the printer. The static outputs of the decade and binary counters (see Figs. 1 and 5) activate triodes whose plate loads are relay coils. After the relays have stored the numbers to be punched (this requires 1/10 second), the rest of the ENIAC may proceed with the computation, while the relays supply signals to the card punch for the actual punching (which requires another 5/10 second).

The card reader can read 120 cards (each holding 80 digits) per minute, and the card punch can punch 100 cards per minute. Thus 960 ten-digit numbers can be supplied to the ENIAC per minute, and 800 ten-digit numbers can be recorded per minute. These input and output speeds are slow, relative to the speed of electronic computation within the machine (300,000 additions per minute, 23,000 multiplications per minute, etc.). Thus the ENIAC is best suited to those problems in which a large amount of computation is done with relatively little data and with relatively few quantities to be recorded. This limitation is accompanied by the restriction that the setup of problems, being manual, is slow; this fact makes the ENIAC best suited to problems in which a large number of iterated solutions are desired. The production of firing tables by repeated solution of the total differential equations of exterior ballistics is a good example of a problem well-matched to the ENIAC input, output, and setup speeds.

Three function tables provide a method of supplying numbers which remain fixed throughout a problem. Each function table holds 104 values of any arbitrary function; these values are set into a function table matrix manually, i.e., by turning switches which interconnect horizontal buses (representing the 104 values of the argument) to vertical buses (representing the digits of the function value) through resistors. When a two-digit number (argument) is sent to a function table, it will produce the corresponding function value (in the form of groups of pulses) in 1/1000 of a second. Though the numbers stored in a function table may represent programming instructions,¹⁵ the chief use of a function table is to store arbitrary functions which have no simple mathematical formulation. As has already been pointed out, the ballistic drag function (stating the resistance of the air to a shell as a function of the shell's velocity) is of this type. A large class of scientific problems are difficult to solve (i.e., the actual solution process is complicated) solely because they involve such arbitrary functions, and hence they are well-adapted for solution on the ENIAC.

Each of the units described above contains, in addition to the circuits required to perform its operations, local programming circuits for controlling these operations. The programming circuits of a unit include a number of "program controls" which function in the following manner. A program control has associated with it some switches by means of which a given operation may

¹⁵ In which case the function table emits program pulses, rather than digit pulses.

be selected; for example, an accumulator program control may be set to "add and clear," or to "receive," etc. (see Section VI-B). When a program control is stimulated by a program pulse, it directs its unit to perform the operation preset on the switches and emits a program pulse when this is completed. This output pulse

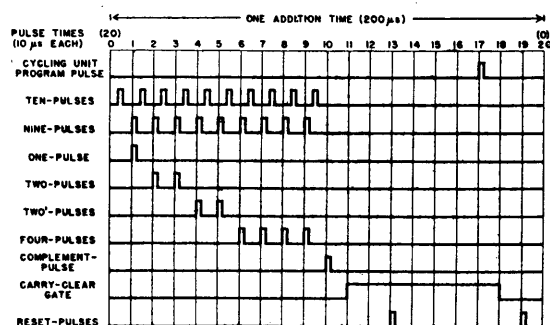


Fig. 6—Cycling-unit pulses.

then goes to the program control (or controls) which directs the next operation in the computation. To set up a problem on the ENIAC, one establishes chains or sequences of local program controls by interconnecting their inputs and outputs and setting the switches associated with them. For example, the following sequences occur in the solution of the exterior ballistic equations: (1) the reading of initial data; (2) the computation of a portion of a known trajectory and automatic comparison with known answers as a check on the ENIAC operation; (3) the integration of the unknown trajectory over one increment of the independent variable (e.g., over $1/10$ of a second), involving a number of subsequences: (a) an interpolation sequence for data read from function tables, and (b) a number of subintegrations (depending upon the complexity of the integration method used); (4) a sequence to determine whether or not the projectile is at the summit or at the ground (in which case its co-ordinates are to be punched on cards); and (5) a punching sequence.

The solution of the exterior ballistic equations clearly requires a repeated use of these different sequences which have been set up on the local program controls, and the number of times that any sequence is to be iterated may be a function of the numbers produced by the arithmetic units (e.g., the integration sequence (3) is followed until the projectile reaches the summit and then the punching sequence (5) is followed, etc.). The over-all control of the sequences (and subsequences, supersequences, etc.) is handled by the master programmer. It contains ten six-stage counters, each of which routes incoming program pulses over any of six different output channels. The positions of these counters may be controlled either by the number of pulses which have been supplied to the various output channels or by pulses received (such as the pulses representing the digit of a number) on a special input terminal. In this way the schedule of sequences may be fixed in advance, or it may be made contingent on the results of the computation.

Although the programming of the ENIAC is completely automatic (once it is set up), it must be initiated by the operator. He accomplishes this by pushing a switch on the initiating unit, which causes a program pulse to initiate the first sequence of operations. When that sequence is finished, the program pulse coming from the last program control circuit used in the sequence is returned to the master programmer, which selects the next sequence to be performed. This process is then repeated until the problem, or set of problems, is completed.

The units of the ENIAC operate as a synchronized system, the operations of each unit being governed by a standard set of timed signals furnished by the cycling unit (see Fig. 6). A fundamental reason for this mode of operation has to do with reliability of operation. In the process of transmission from circuit to circuit, electrical pulses suffer degeneration both in amplitude and in phase. If pulses were retransmitted from one circuit to another, etc., progressive degeneration might result and adversely affect the reliability of operation. Transmitted pulses are thus always derived by gating pulses received from the cycling unit.

The ten different kinds of pulses produced by the cycling unit and transmitted to all other units are derived from a master oscillator which normally operates at 100,000 cycles per second, but which may be operated at other frequencies for checking and fault-detecting purposes. The pulses from the oscillator are used to step a twenty-stage ring counter and are (after passing through an electrical delay line) in turn gated by gate tubes operated by this counter. All pulses are of the same phase except the ten-pulses; they are shifted by being passed through another electrical delay line. All pulses are of about two microseconds duration (except for the carry-clear gate) and about fifty volts magnitude.

In the normal operation of the ENIAC, the cycling unit transmits these pulses to all other units continuously; the actual course of the computation is then controlled by the programming circuits. For purposes of checking a setup and localizing a fault, however, two discontinuous types of operation of the cycling unit are provided for. These are called the one-addition-time and one-pulse-time modes of operation and are selected by means of a manual switch. In the one-addition-time mode of operation, the cycling unit emits the complete set of pulses shown in Fig. 6 once every time a push button is pressed and then stops; but the pulses emitted have the same shape, duration, and spacing as during continuous operation, so that the operation of the ENIAC units during this 200-microsecond period is normal. All ENIAC circuits are designed so that they retain their information whenever the cycling unit stops. (This partly accounts for the large number—80—of direct-voltage levels in the ENIAC). By this means a problem can be solved by one-addition-time steps; the numbers and programming signals held in the flip-flops can be read by means of neon bulbs and the operation

checked in that manner. When the error is localized to within a given addition time, the one-pulse-time mode of operation is used. This results in the cycling-unit counter's advancing one stage each time the push button is pressed, so that the signals for a given ten-micro-second period are emitted. In this way, the fault can be isolated to within a group of from one to about a dozen tubes.

VI. ANALYSIS OF TYPICAL CIRCUITS

In this section we will show how the basic circuit elements discussed in Sections III and IV are combined to form computing circuits. The accumulator decade circuit (Fig. 2) will show how a counter is used for addition and subtraction, the program control circuit of an accumulator (Fig. 3) will show how a local programming circuit governs the operation of its unit, and the multiplication circuit (Figs. 4 and 7) will show how a function table is employed in high-speed multiplication.

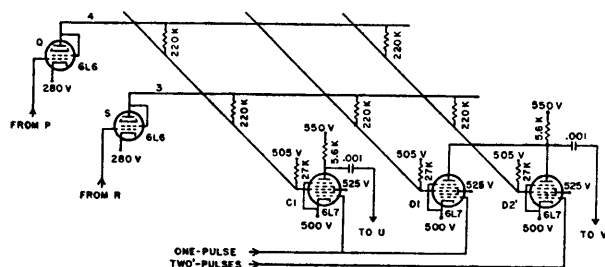


Fig. 7—Cross section of multiplication table.

A. Accumulator Decade Circuit

Each accumulator contains ten decade circuits like that of Fig. 2, in addition to a sign circuit (which uses the binary counter of Fig. 5 to store the sign of the number) and the programming circuits (of which Fig. 3 is a sample). Each decade counter stores a single decimal digit and adds to its contents a digit received in the form of pulses. Incoming pulses are first shaped by tubes 3, 4, and 5 (see tubes 1, 2, and 3 of Fig. 5 for the circuit) and then supplied by tube 6 to the counter.¹⁶ Tubes 9, 10, 11, and 12 are connected as a flip-flop, called the carry flip-flop, which remembers whenever a carry takes place during the reception of a number and is used during transmission to control gates 13 and 14.

The addition of two numbers requires the simultaneous operation of the decades of two accumulators. The decades of the transmitting accumulator convert the digits held in them into groups of pulses which are transmitted to the receiving accumulator. The decades of the receiving accumulator receive these pulses and add them to their contents. We will discuss first the operation of the circuit of Fig. 2 when it is receiving a number arriving in pulse form on a digit trunk. Since

¹⁶ Tube 6 is the 6L6 driving tube shown in Fig. 1. The clearing tube and clearing connections of the counter of Fig. 1 are not shown in Fig. 2, and only one static output lead (that coming from stage 9) is shown.

these digit pulses have been derived from the cycling-unit digit pulses (the nine-pulses, the one-pulse, the two-pulses, the two'-pulses, the four-pulses, and the complement pulse), they will arrive during pulse times one to ten inclusive.

When the problem is set up, one input of gate tube 2 is connected to a digit trunk. Since the same digit trunk is used by other ENIAC units, a gate tube is required here so that pulses passing over this digit trunk do not go into the decade counter, except during those addition times when the other input of gate tube 2 is opened by a signal from the programming circuits. As an example, suppose that the decade counter registers 8 and that five pulses pass over the digit trunk while gate tube 2 is open. These pulses pass through gate tube 2 to the pulse standardizer (tubes 3, 4, and 5), and thence into the counter, counting it from 8 around through 9 and 0 and up to 3. Since 5 plus 8 makes 13, i.e., 3 with 1 to carry, one pulse should have been supplied to the decade to the left when the counter went from 9 to 0. But since that decade may also be receiving pulses from the digit trunk during this period of time, the fact that a carry-over took place must be remembered, and the carry pulse sent to the next decade to the left later in the addition time. This fact is remembered by the carry flip-flop and the carrying is done during pulse times eleven to seventeen inclusive.

The method of setting the carry flip-flop when the counter passes from 9 to 0 is of some interest, since it illustrates the design rule (mentioned in Section V) that pulses are never generated in ENIAC units but are derived from cycling-unit pulses by means of gating circuits. The pulse for setting the carry flip-flop could have been taken from the number 9 stage of the counter except for this rule, for the number 9 stage gives out a pulse as the counter goes from 9 to 0. Instead, gate tube 7 was added. This gate tube receives every incoming pulse from tube 5 of the pulse standardizer on one input, and is turned "on" on the other input when the counter registers a 9. Thus when a counter registers a 9, the pulse which steps the counter to 0 also goes through gate tube 7 and sets the carry flip-flop, electronically recording the fact that a carry has occurred. (The pulse from tube 7 also goes through inverter tube 22 and to gate tube 24, but it is blocked here since the cycling unit carry-clear gate is not on during pulse times one to ten.) Thus, at the end of pulse time ten, each counter holds the sum of its original digit and the digit received (modulo 10), and each carry flip-flop records whether or not a carry took place.

The carrying takes place during pulse times eleven to seventeen, (i.e., after all possible pulses have arrived from the digit trunk). During this period, the carry-clear gate from the cycling unit is passed by the accumulator program controls through to gates 23 and 24, opening them up. At pulse time thirteen the first reset-pulse is applied to gate tube 8, which is open since (in this example) the carry flip-flop is set. The reset-pulse then

passes through tube 8, resets the carry flip-flop (so it will be ready for the next operation), and goes through inverter 21 and gate tube 23 into the next decade to the left. In this way, the carry-over is effected.

One such carry-over may give rise to another carry-over, and this to another, etc.; for if a decade receiving a carry-pulse already holds a 9, a further carry must take place. This is accomplished by means of tubes 7, 22, and 24. Suppose, for an example, that the counter of Fig. 2 is registering 9 when a carry-pulse enters the pulse standardizer from the decade to the right. Since the counter is on stage 9, gate tube 7 is open, so that this pulse (in addition to stepping the counter from 9 to 0) passes through tubes 7, 22, and 24 and into the next decade. (This pulse will also set the carry flip-flop; the carry flip-flop is reset by the second reset-pulse at pulse time nineteen, i.e., after the carry-clear gate has gone, so that the pulse generated in this resetting process is blocked at gate 23.)

One may wonder why the carry-clear gate is on for fifty microseconds after the first reset-pulse initiates the carry-over. The reason for this is that in an extreme case twenty carry-overs may take place in sequence. Consider, for instance, the addition of $+1$ to -1 , the numbers being stored in twenty-digit accumulators.¹⁷ A negative number, such as -1 , is stored as a complement, that is, -1 is stored as $M99,999,999,999,999,999,999$, where the " M " means that the binary sign counter registers "minus." When the number $+1$ is added to the contents of this accumulator, 1 pulse is sent to the units decade and no pulses to any other decade. The single pulse going into the units decade counter will change it from a 9 to a 0 and set its carry flip-flop. When the carry-over is initiated, the first reset-pulse goes through tubes 8, 21, and 23 of the units decade into the tens decade; since the tens decade holds 9, this pulse goes on (after being reshaped by the pulse standardizer) through tubes 7, 22, and 24 of the tens decade into the hundreds decade; this process is then repeated for a total of twenty times, until the pulse has changed all decades from 9 to 0 (except the units decade, already at 0) and the binary sign counter from M to P , thus leaving the number 0 in the accumulator ($1-1=0$!). Experimental measurement showed that about twenty-five microseconds were required for such a complete twenty-place carry, so (to provide a two-to-one safety factor) fifty microseconds are allowed by the cycling unit.

Let us next consider the operation of the circuit of Fig. 2 during the transmission of a number. The problem here is to convert the number statically registered in the decade counter into pulse form. When addition takes place, the number of pulses emitted (through tube 16 and buffers 19 and 20) is equal to the digit held in the counter. When subtraction takes place, the number of

pulses emitted (through tube 15 and buffers 17 and 18) is equal to the difference between the digit and 9.¹⁸ Thus if the counter of Fig. 2 holds the digit 3, three pulses are transmitted from the addition output and six pulses from the subtraction output.

This could have been accomplished by connecting gate tubes to the static outputs of the counter and supplying the proper sets of pulses to these gates. (For example, the add gate connected to the third stage would be supplied with three pulses and the subtract gate with six pulses.) A method more economical of tubes is employed, however. It makes use of the ten-pulses from the cycling unit. These are introduced into the decade during the transmission process through buffer tube 1. They cycle the counter completely around through 9 and 0 and up to where it was at the beginning; that is, from 3 to 9 and 0 and to 3 again in the example we are considering. As the counter goes from 9 to 0, the carry flip-flop is set; this occurs during pulse time six in our example. Before the carry flip-flop is set the subtract gate (tube 13) is open, while after it has been set the add gate (tube 14) is open. Thus, in this example, the subtract gate is open from the middle of pulse time zero to the middle of pulse time six, while the add gate is open from the middle of pulse time six to the middle of pulse time nine. Hence, if the nine pulses from the cycling unit are supplied to the subtract gate during this addition time, six of them will be passed; whereas if they are supplied to the add gate, three of them will be passed. In this way the nine pulses are divided into two groups, one representing the digit stored in the decade at the beginning of the process, and the other representing the complement of that digit with respect to 9. The decade is left in its initial position (since no carry-overs are allowed to take place) and the carry flip-flop is reset at the end of the process (by the reset pulses). The digit pulses are transmitted onto digit trunks by means of the cathode-follower buffer tubes 17, 18, 19, and 20.

B. Program Control Circuit

As already stated, the various units of the ENIAC have local programming circuits which govern the operation of these units. At the particular time when a unit is to be used, a program pulse (derived from the cycling-unit program pulse and hence coming during pulse time 17) is sent to a program control of that unit. The program control selected causes the unit to perform the predetermined operation (set up on switches), and then emits a program pulse which is sent to another unit (or units) via a program line to cause the next operation in the sequence to be performed.

Fig. 3 is a somewhat simplified circuit of an accumulator program control. An accumulator has twelve pro-

¹⁸ The taking of complements is achieved by complementing each digit with respect to 9 (i.e., taking the difference between that digit and 9) and adding one pulse in the units place, so that the units digit is effectively complemented with respect to 10. The cycling-unit complement-pulse is used for this extra pulse.

¹⁷ It will be remembered that two accumulators may be interconnected so as to form a twenty-digit accumulator.

gram controls, on each of which may be set up a particular operation, e.g., add and clear, receive a number, subtract without clearing, etc., and each of which is used at a different time during the computation. All program controls operate certain common programming circuits, which in turn cause the decade circuits and sign circuit to act. For example, program control number 3 may direct the accumulator to receive at one point during a computation, and program control number 5 may direct the accumulator to receive at a different time. Since either program control must be able to control reception without the other's being affected, both are connected through buffers (such as tube 7 of Fig. 3) and switches (so that the operation can be selected manually in the setup of a problem) to the common programming circuits which, when stimulated by either program control, will open gate tube 2 and will pass the cycling-unit carry-clear gate to gate tubes 23 and 24 of Fig. 2.

Let us trace through the operation of the circuit of Fig. 3 from the time it receives a program pulse to the time it emits such a pulse. A positive program pulse received on the input terminal of the program control is amplified by tube 5 and sets the flip-flop (tubes 1, 2, 3, and 4). The flip-flop static outputs operate buffer tubes 7 (through amplifier tube 6) and 8 and one input of gate tube 9. Buffer tube 7 connects through a switch to the common circuits which may be operated by the buffer tubes of any program control; the setting of the switch controls whether the operation is transmission, additively or subtractively, or reception. Buffer 8 connects through a clear switch to the circuits which cause the accumulator to be cleared. The load resistors for these buffers are located in the common circuits.

Gate tube 9 receives the cycling-unit program pulse on the first grid every addition time. Hence, when its other input is activated by the flip-flop, it passes the pulse to transmitter tubes 10 and 11¹⁹ and to the flip-flop, causing it to be reset. Thus, the program control emits a program pulse (which will go to stimulate the next operation in the sequence of operations) and is left in the reset condition (so that it may be used again when that sequence is repeated).

There is a timing problem in this operation which should be noted. As soon as the flip-flop is set by the program pulse coming from another program control, (and hence derived from the cycling-unit central program pulse) gate 9 will be opened. But if this action occurred within two microseconds (the duration of a pulse), the same cycling-unit program pulse from which the input was derived would be passed by gate 9, and the flip-flop would be reset immediately. This is prevented by means of capacitor C_3 (300 micromicrofarads), which slows up the operation of the circuit.

¹⁹ The load resistor for tube 11 is not located in the program control, but is attached to the program line running around the front of the machine, since the number of such buffer tubes which are connected together to a given program line depends upon the particular problem set up on the ENIAC.

One further point of circuit design should be discussed. It will be noted that the grid of every conducting tube is driven positive. Thus, the grid of tube 10 normally draws about one-third milliampere of grid current, and when the flip-flop is set, the grids of tubes 8 and 9 are driven positive, with respect to the cathodes of these tubes. The purpose of this mode of operation is to increase the plate current of conducting tubes (and thus decrease the effective plate resistance), to reduce the effect of spurious signals picked up on the leads (since the gain of the tube is decreased when the grid is positive), and to make sure that the driven stage is operated, even if the driving tube is not completely turned off (and hence is drawing some plate current). The last factor is especially important in the high-speed multiplier, where twenty-four buffers (normally nonconducting tubes) are connected in parallel to a common load resistor.

C. Multiplication Circuit

In most problems, multiplication is the chief factor determining the duration of the computation. Though multiplication occurs less frequently than addition (a typical problem will have one multiplication for every four additions), it is a more lengthy process because it involves a number of additions. If multiplication is done by successive additions in sequence, a maximum of ninety addition times would be required for ten-digit numbers. To increase the over-all speed of computation within the ENIAC, it was decided to use a process of multiplication faster than that of successive additions, even at the cost of complicating the multiplier somewhat. The process chosen makes use of an electrical multiplication table; by means of it the complete multiplicand can be multiplied by a single digit of the multiplier in one addition time.

A description of the operation of the circuits of the high-speed multiplier, capable of handling ten-digit numbers, is too complicated for us to give here. Instead, we will consider a simplified version of the circuit, as shown in Fig. 4. The circuit of Fig. 4 can handle only two-digit multipliers and multiplicands (and hence will produce only four-digit products). Moreover, to effect further simplification, only part of the multiplication table is shown (and hence only some of the output gates), namely, that part used by multiplicand digits of one, two, or three. Thus, in our example, we will take a multiplicand of which neither digit exceeds three.

Tubes A0 through A9 and B0 through B9 form what is called the multiplier selector since, by means of this array of tubes, one digit of the multiplier can be selected at a time. On one input these gate tubes are connected in one-one correspondence with the static outputs of the stages of the decade counters of the accumulator holding the multiplier (called the multiplier accumulator). On the other input these gate tubes are connected in columns to lines coming from the programming circuits (lines 1 and 2). These lines are activated in sequence

(one each addition time) so that one digit of the multiplier is selected at a time. The outputs of the selector gates are connected in rows to drive the multiplication table (through tubes *P*, *Q*, *R*, *S*, etc.).

The digit selected operates the multiplication table and associated output gates (the tubes lettered *C*, *D*, *E*, *F*, and *G*). The table is so wired up that when the incoming bus representing a digit from 0 to 9 is activated, all output gate tubes are turned off except those representing the products of that digit by the digits from 0 to 9. The output gate tubes are pulsed with pulses from the cycling unit, so that the whole network generates the products of the multiplier digit selected by *all* digits from 0 to 9. Since the product of two single-digit numbers is in general a two-digit number, the multiplication table is divided into two parts, the left-hand part (producing the tens digit of the product) and the right-hand part (producing the units digit of the product). For example, if the multiplier digit is 7, tube *D2'* will pass two pulses and tube *G1* will pass one pulse, since the product of 7 times 3 is 21, i.e., 2 in the tens place and 1 in the units place.

The units and tens outputs of the multiplication table are fed into two multiplicand selectors, called the left-hand multiplicand selector (the tubes lettered *H* and *J*) and the right-hand multiplicand selector (the tubes lettered *K* and *L*). Each selector consists of an array of gate tubes (certain rows are not needed) connected on one input in one-one correspondence with the static outputs of the stages of the decimal counters of the accumulator holding the multiplicand (called the multiplicand accumulator). On the other input these gate tubes are connected in rows to the lines coming from the multiplication table output gates (via inverters *U*, *V*, etc.), each row receiving pulses according to the digit it represents. Thus tubes *H3* and *J3* represent possible multiplicand digits 3 and hence receive pulses from the number 3 channel of the left-hand part of the multiplication table (from tubes *D1* and *D2'*). The outputs of the selector gates are connected in columns and go to the shifters.

The electronic shifters (the tubes lettered *M* and *N*) consist of square arrays of gate tubes used to shift the partial products into position. On one input the gates of a shifter are connected together in columns which receive the outputs of the corresponding multiplicand selector. On the other input the gates of a shifter are connected to the lines coming from the programming circuits which are activated in sequence, one being on for each successive multiplier digit (lines 1 and 2). The outputs of a shifter are connected together diagonally, so that the pulses coming out of the shifter are moved over one place each time a different multiplier digit is used.

Suppose, for example, that the multiplier is 76 and the multiplicand is 21. As a consequence, one input of each of the following selector tubes is activated: *A7*, *B6*, *H2*, *K2*, and *L1*. The programming circuits energize line 1 and as a result two things happen. First, gate tube *B6*

goes on, causing the number 6 line of the multiplication table to be energized; this causes gate tubes *D2'*, *E1*, *E2'*, *F2'*, *F4*, and *G1* to be turned off—the remaining tubes pass the pulses received from the cycling unit. Second, the shifter gate tubes *M1*, *M2*, *N1*, and *N2* are activated on one input. The pulses coming from the multiplication table (representing the product of 6 times 1, 2, and 3) go to the multiplicand selectors. Tube *H2* passes the one pulse received from the table, and tubes *K2* and *L1* pass 2 and 6 pulses, respectively. Thus pulses are emitted by the left-hand multiplicand selector representing 10, and pulses come from the right-hand selector representing 26. These come out of the shifters as 0100 and 0026 and go to the accumulators which collect the partial products.

The program controls activate line 2 during the next addition time, the multiplier digit 7 is selected, and pulses come out of the shifters representing 1000 and 0470 and go into the left-hand and right-hand partial products accumulators (producing the sums 1100 and 0496, respectively). After all of the multiplier digits have been used in this manner, corrections are made in case negative numbers (complements) are involved, and the left-hand partial products are then added to the right-hand partial products, producing the final answer.²⁰ In the example we have taken, the final sum will be 1596, which is the product of 76 and 21.

A more detailed view of one section of the multiplication table is shown in Fig. 7. When the table is in operation, the buses representing all the digits except the one selected are positive; the one selected is driven negative, turning off those output gate tubes which are connected to the selected bus through the 220,000-ohm resistors. Of course, because of the cross-connections via the various 220,000-ohm resistors, the nondriven buses will receive a certain amount of negative signal, and this will, in turn, have a tendency to turn off the gate tubes which are supposed to be on. This "parasitic" signal is overcome by driving the grids positive (the grid resistors go to 505 volts, whereas the cathodes are held at 500 volts). The design of the table must take into account the possible parasitic signals. These are a function of the matrix of connections and the resistances of the driving tubes, the cross-connecting resistors, and the grid resistors. The problem was particularly acute in the case of the tables used in the function tables, both because these were so large (over one hundred buses on each side), and because the matrix connections are variable; the parasitic signal was decreased in that case and the operating signal made less dependent upon the particular matrix connections set up by using plate load resistors in parallel with the load provided by the table itself. The multiplication table has, of course, fixed connections. It was further simplified by the use of a coded system; instead

²⁰ These operations take two addition times. At the beginning of the multiplication, an addition time is required for setting up the selector circuits. Hence, the multiplication of ten-digit numbers takes 13 addition times or 2.6 milliseconds.

of having an output gate tube for each digit from 1 to 9, gate tubes receiving the one-pulse, the two-pulses, the two'-pulses, and the four-pulses were used. This required fewer output gate tubes and made possible a better-balanced multiplication table.

VII. CONCLUSION

Since its dedication on February 15, 1946, the ENIAC has produced results of great value in both theoretical and applied fields, demonstrating unquestionably that electronic computation is practicable. Except for an initial period of testing, the rate of failures has been

only about two or three per week, most failures being caused by heater-cathode short circuits and heater open circuits in tubes. These can usually be detected, localized, and corrected quickly, despite the complexity of the ENIAC, by an operator who is thoroughly familiar with all the details of ENIAC design and with the particular problem being solved. Under such an operator only a few hours per week are lost on account of failures.

Because the ENIAC combines the desirable features of speed and reliability, it is capable of solving problems hitherto beyond the scope of science. Thus it inaugurates a new era, an era of electronic computation.