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PMIC with Ultra-Low I_Q Voltage Regulators, Buck-Boost for Optical Sensing and Charger for Small Lithium Ion Systems

MAX20345

General Description

The MAX20345 is a power management solution featuring ultra-low I_Q voltage regulators, ideal for low-power wearable applications. The device includes a linear battery charger with a smart power selector and several power-optimized peripherals. The device features three buck regulators, three low-dropout (LDO) linear regulators, and a Buck-Boost regulator, providing up to seven regulated voltages, each with an ultra-low quiescent current. Two load switches allow disconnecting system peripherals to minimize the total quiescent load of the system. MAX20345 allows system designers to minimize power consumption and extend battery life in 24/7 operation devices, such as those in the wearable market.

The three synchronous, high-efficiency buck regulators use a pulse frequency modulated (PFM) control scheme for increased efficiency during light-load operation. The output voltage of these regulators can be programmed through I^2C down to voltages as low as 0.7V. Additionally, the buck regulators support dynamic voltage scaling (DVS) allowing the system designer to further improve system power consumption when using devices that can take advantage of DVS.

Each of the three LDO regulators output voltage can be programmed through I^2C. For additional flexibility, each LDO can be configured as a load switch that can be used to disconnect the quiescent load of the system peripherals.

The integrated Buck-Boost converter provides a convenient way to power system peripherals that require voltages higher and/or lower than the battery voltage, and is optimized for optical sensing systems such as optical heart rate (OHR)/PPG and SpO_2 measurements. The output noise of the Buck-Boost is minimized to provide the least impact possible on sensitive measurements in such systems. The addition of DVS offers further power savings during favorable measurement conditions.

The MAX20345 also features a programmable power controller that allows the device to be configured for applications that require the device be in a true-off, or always-on, state. The controller provides a delayed reset signal and voltage sequencing. The MAX20345 is available in a 56-bump, 0.4mm pitch, 3.37mm x 3.05mm wafer-level package (WLP).

Applications

- Wearable Devices
- IoT

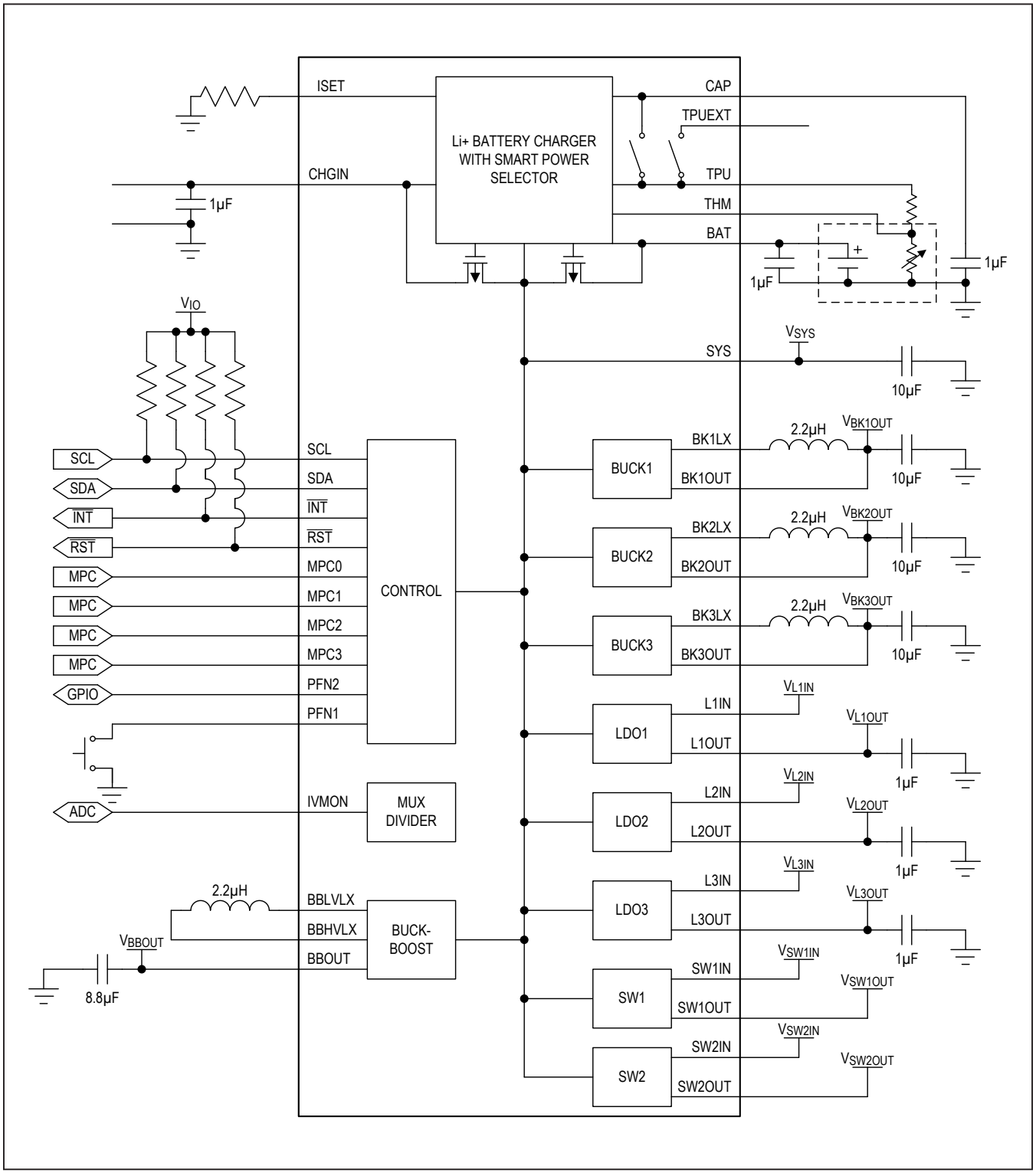
Benefits and Features

- Extend Battery-Use Time Between Charging
  - 3 x Low I_Q Buck Regulators (I_Q = 0.9µA typ)
    - 220mA Output Current
    - Noise Mitigation by Flexible Adjustment of Switching Frequency
    - Buck1: 0.700V to 1.330V Output Voltage in 10mV Steps
    - Buck2: 0.700V to 2.275V Output Voltage in 25mV Steps
    - Buck3: 0.700V to 3.850V Output Voltage in 50mV Steps
  - LDO1 (I_Q = 0.55µA typ)
    - 100mA Output
    - 2.7V to 5.5V Input Voltage Range
    - 0.8V to 3.6V Output Voltage in 100mV Steps
  - LDO2 (I_Q = 1µA typ)
    - 100mA Output
    - 1.71V to 5.50V Input Voltage Range
    - 0.9V to 4.0V Output Voltage in 100mV Steps
  - LDO3 (I_Q = 1µA typ)
    - 50mA Output
    - 1.00V to 2.00V Input Voltage Range
    - 0.50V to 1.95V Output Voltage in 25mV Steps
  - 2 x Load Switches
    - 0.65V to 5.50V Input Voltage Range
    - 1Ω R_{ON} at SYS = 3.0V
  - Low I_Q Buck-Boost Regulator (I_Q = 2µA typ)
    - 1.5W Output Capability
    - 2.6V to 5.5V Output Voltage in 50mV Steps
- Easy to Implement Li+ Battery Charging
  - Linear Li-Ion Battery Charger
    - 5mA to 500mA Charge current
    - +28V / -5.5V Tolerant Input
    - Step Charging (See the *Step Charging* Section)
  - Thermistor Monitor
  - Smart Power Selector
- Optimize System Control
  - Power On/ Reset Controller
  - Push-Button Monitor
  - Factory Shipping Mode
  - System Interface
    - Monitor Multiplexer with Programmable Divider to Monitor System Voltages and Charging Current

Ordering Information appears at end of data sheet.

19-100366; Rev 11; 9/23

Functional Diagram



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Absolute Maximum Ratings

(Voltages referenced to GND)
CHGIN .....-6.0V to +30.0V
SDA, SCL, THM, $\overline{RST}$, SYS, PFN_, $\overline{INT}$, IVMON, BAT, L1IN, L2IN, BBOUT, SW_IN, TPUEXT, TPU .....-0.3V to +6.0V
CAP ..... -0.3V to min ($|V_{CHGIN}|$ + 0.3V, +6.0V)
L3IN .....-0.3V to 2.2V
MPC_, BK_LX, BK_OUT, BBLVLX..... -0.3V to (V_{SYS} + 0.3V)
BBHVLX .....-0.3V to min (V_{BBOUT} + 0.3V, +6.0V)
ISET.....-0.3V to min (V_{BAT}, V_{SYS} + 0.3V)
L_OUT .....-0.3V to (V_{L_IN} + 0.3V)
LSW_OUT .....-0.3V to (V_{LSW_IN} + 0.3V)

Continuous Current into
CHGIN, BAT, SYS .....±1000mA
Continuous Current into
Any Other Terminal.....±100mA
Continuous Power Dissipation (multilayer board at +70°C):
8 x 7 Array 56-Ball, 3.37mm x 3.05mm 0.4mm Pitch WLP
(derate 24.79mW/°C)..... 1115.5mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 56 WLP	
Package Code	W563H3+1
Outline Number	**21-100260**
Land Pattern Number	**Refer to Application Note 1891**
THERMAL RESISTANCE, FOUR-LAYER BOARD:	
Junction to Ambient (θ_{JA})	40.35°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GLOBAL SUPPLY CURRENT						
CHGIN Input Current	I_{CHGIN}	V_{CHGIN} = 5V, on state, charger disabled, battery thermal monitoring disabled, all rails disabled		0.72	1.20	mA
BAT Input Current	I_{BAT}	V_{CHGIN} = 0V, off state, LDO1 disabled		0.40	0.96	µA
		V_{CHGIN} = 0V, off state, LDO1 enabled, L1IN connected to BAT		1.10	2.20	
		V_{CHGIN} = 0V, on state, all rails disabled		1.45	2.50	
		V_{CHGIN} = 0V, on state, Buck1 enabled, V_{BK1OUT} = 0.9V		2.30	3.70	
		V_{CHGIN} = 0V, on state, Buck1 enabled, Buck2 enabled, V_{BK1OUT} = 0.9V, V_{BK2OUT} = 1.2V		2.75	4.30	
		V_{CHGIN} = 0V, on state, Buck1 enabled, Buck2 enabled, Buck3 enabled, V_{BK1OUT} = 0.9V, V_{BK2OUT} = 1.2V, V_{BK3OUT} = 1.8V		3.20	5.00	
		V_{CHGIN} = 0V, on state, all rails enabled, LDOs in LDO mode, load switch voltage protection enabled, V_{BK1OUT} = 0.9V, V_{BK2OUT} = 1.2V, V_{BK3OUT} = 1.8V, V_{BBOUT} = 4V		9.00	14.30	
UVLOS AND BAT OCP						
VCCINT UVLO Threshold (POR)	V_{VCCINT_UVLO}	Rising (Note 2)	2.25	2.45	2.80	V
		Falling (Note 2)	2.20	2.40	2.70	
VCCINT UVLO Threshold (POR) Hysteresis	$V_{VCCINT\_UVLO\_H}$	(Note 2)		50		mV
Internal CAP Regulator	V_{CAP}	V_{CHGIN} = 4.3V to 28V	3.75	4.10	4.55	V
CAP Detect Threshold	V_{CAP_DET}	V_{CHGIN} = V_{CAP} rising	3.15	3.40	3.60	V
		V_{CHGIN} = V_{CAP} falling	2.60	2.80	3.00	
CAP Detect Threshold Hysteresis	$V_{CAP\_DET\_H}$			600		mV
CHGIN Detect Threshold	V_{CHGIN_DET}	Rising	4.00	4.15	4.30	V
		Falling	3.20	3.30	3.40	
CHGIN Detect Threshold Hysteresis	$V_{CHGIN\_DET\_H}$			850		mV

Electrical Characteristics (continued)

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CHGIN Detection Debounce Time	t_{CHGIN_DET}	CHGIN insertion			108		ms
		CHGIN detachment			100		
SYS UVLO Threshold	V_{SYS_UVLO}	Rising		2.65	2.75	2.85	V
		Falling		2.60	2.70	2.80	
SYS UVLO Threshold Hysteresis	$V_{SYS\_UVLO\_H}$				50		mV
SYS UVLO Falling Debounce Time	$t_{SYS\_UVLO\_FDEB}$	SYS Falling			20		µs
BATOC Threshold Accuracy	$I_{BAT\_OC\_ACC}$	From 200mA to 1.6A in 200mA steps, device specific (see IBatOc in Table 3)		-40		+40	%
BATOC Threshold Hysteresis	$I_{BAT\_OC\_H}$				6		%
BATOC Rising Debounce Time	$t_{BAT\_OC\_D}$	BAT load current rising			50		ms
OVP AND INPUT CURRENT LIMITER							
CHGIN Overvoltage Threshold	V_{CHGIN_OV}			7.2	7.5	7.8	V
CHGIN Overvoltage Threshold Hysteresis	$V_{CHGIN\_OV\_H}$				200		mV
CHGIN Valid Trip Point	$V_{CHGIN\_SYS\_TP}$	V_{CHGIN} - V_{SYS} rising		30	145	290	mV
CHGIN Valid Trip Point Hysteresis	$V_{CHGIN\_SYS\_TP\_H}$				275		mV
Input Overcurrent Max Limit	I_{LIM_MAX}	Device Specific (see Table 3)	$t < t_{ILIM\_BLANK}$, ILimMax = 0.	400	450	500	mA
			$t < t_{ILIM\_BLANK}$, ILimMax = 1.	900	1000	1100	
Input Current Limit	I_{LIM}	ILimCntl = 000			50		mA
		ILimCntl = 001		80	90	100	
		ILimCntl = 010			150		
		ILimCntl = 011			200		
		ILimCntl = 100			300		
		ILimCntl = 101			400		
		ILimCntl = 110		400	450	500	
		ILimCntl = 111		900	1000	1100	
Input Current Limit Blanking Time	t_{ILIM_BLANK}	ILimBlank = 00			0.0		ms
		ILimBlank = 01			0.5		
		ILimBlank = 10			1.0		
		ILimBlank = 11			10.0		

Electrical Characteristics (continued)

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYS Regulation Voltage	V_{SYS_REG}			V_{BAT_REG} + 0.14	V_{BAT_REG} + 0.20	V_{BAT_REG} + 0.26	V
SYS Regulation Voltage Dropout	V_{CHGIN_SYS}				40		mV
CHGIN to SYS On-Resistance	R_{CHGIN_SYS}				0.37	0.66	Ω
Input Current Soft-Start Time	t_{ILIM_SFT}				1		ms
Thermal Shutdown Temperature	T_{CHG_SHDN}	Device Specific (see Table 3)	TShdn = 000		50		°C
			TShdn = 001		60		
			TShdn = 010		70		
			TShdn = 011		80		
			TShdn = 100		90		
			TShdn = 101		100		
			TShdn = 110		110		
			TShdn = 111		120		
CHGIN Boot Retry Timeout	$t_{CHG\_RETRY\_TMO}$	ChgAlwTry = 1			0.5		s
BATTERY CHARGER							
BAT-to-SYS On-Resistance	R_{BAT_SYS}	V_{BAT} = 4.2V, I_{BAT} = 300mA			80	140	mΩ
Thermal Regulation Temperature	T_{CHG_LIM}				T_{CHG_SHDN} - 3		°C
BAT-to-SYS Switch On Threshold	$V_{BAT\_SYS\_ON}$	SYS falling, measured as V_{BAT} - V_{SYS}		10	19	35	mV
BAT-to-SYS Switch Off Threshold	$V_{BAT\_SYS\_OFF}$	SYS rising, measured as V_{BAT} - V_{SYS}		-3.0	-1.5	0.0	mV
SYS-to-BAT Charge Current Reduction Threshold	$V_{SYS\_BAT\_LIM}$	Measured as V_{SYS} - V_{BAT}, SysMinVlt = 000, V_{BAT} > 3.6V			100		mV
Minimum SYS Voltage	V_{SYS_LIM}	V_{BAT} < 3.4V	SysMinVlt = 000		3.6		V
			SysMinVlt = 001		3.7		
			SysMinVlt = 010		3.8		
			SysMinVlt = 011		3.9		
			SysMinVlt = 100		4.0		
			SysMinVlt = 101		4.1		
			SysMinVlt = 110		4.2		
			SysMinVlt = 111		4.3		
Charger Current Soft-Start Time	t_{CHG_SOFT}				1		ms

Electrical Characteristics (continued)

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Precharge Current	I_{PCHG}	IPChg = 00			0.05 x I_{FCHG}		mA
		IPChg = 01		0.09 x I_{FCHG}	0.10 x I_{FCHG}	0.11 x I_{FCHG}	
		IPChg = 10			0.20 x I_{FCHG}		
		IPChg = 11			0.30 x I_{FCHG}		
Precharge Threshold	V_{BAT_PCHG}	VPChg = 000			2.10		V
		VPChg = 001			2.25		
		VPChg = 010			2.40		
		VPChg = 011			2.55		
		VPChg = 100			2.70		
		VPChg = 101			2.85		
		VPChg = 110			3.00		
		VPChg = 111			3.15		
Precharge Threshold Hysteresis	$V_{BAT\_PCHG\_H}$				90		mV
Step-Charge Threshold	V_{BAT_STPCHG}	V_{BAT} rising	ChgStepRise = 0000		3.80		V
			ChgStepRise = 0001		3.85		
			ChgStepRise = 0010		3.90		
			ChgStepRise = 0011		3.95		
			ChgStepRise = 0100		4.00		
			ChgStepRise = 0101		4.05		
			ChgStepRise = 0110		4.10		
			ChgStepRise = 0111		4.15		
			ChgStepRise = 1000		4.20		
			ChgStepRise = 1001		4.25		
			ChgStepRise = 1010		4.30		
			ChgStepRise = 1011		4.35		
			ChgStepRise = 1100		4.40		
			ChgStepRise = 1101		4.45		
			ChgStepRise = 1110		4.50		
			ChgStepRise = 1111		4.55		

Electrical Characteristics (continued)

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Step-Charge Threshold Hysteresis	$V_{BAT\_STPCHG\_H}$	ChgStepHyst = 000		100		mV
		ChgStepHyst = 001		200		
		ChgStepHyst = 010		300		
		ChgStepHyst = 011		400		
		ChgStepHyst = 100		500		
		ChgStepHyst = 101		600		
Fast Charge Current Reduction Due to Step-Charge	I_{FCHG_STPCHG}	ChgIStep = 000		I_{FCHG} x 0.2		mA
		ChgIStep = 001		I_{FCHG} x 0.3		
		ChgIStep = 010		I_{FCHG} x 0.4		
		ChgIStep = 011		I_{FCHG} x 0.5		
		ChgIStep = 100		I_{FCHG} x 0.6		
		ChgIStep = 101		I_{FCHG} x 0.7		
		ChgIStep = 110		I_{FCHG} x 0.8		
		ChgIStep = 111		I_{FCHG}		
ISET Current Gain Factor	K_{ISET}			2000		A/A
ISET Regulation Voltage	V_{ISET}			1		V
BAT Fast Charge Current Set Range	I_{FCHG}	R_{ISET} = 400kΩ		5		mA
		R_{ISET} = 40kΩ	45	50	55	
		R_{ISET} = 4kΩ		500		

Electrical Characteristics (continued)

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Battery Regulation Voltage	V_{BAT_REG}	BatReg = 0000		4.050		V
		BatReg = 0001		4.100		
		BatReg = 0010		4.150		
		BatReg = 0011, T_A = 25°C	4.179	4.200	4.221	
		BatReg = 0011	4.158	4.200	4.242	
		BatReg = 0100		4.250		
		BatReg = 0101		4.300		
		BatReg = 0110		4.350		
		BatReg = 0111		4.400		
		BatReg = 1000		4.450		
		BatReg = 1001		4.500		
		BatReg = 1010		4.550		
		BatReg = 1011		4.600		
Battery Recharge Threshold	V_{BAT_RECHG}	BatReChg = 00		70		mV
		BatReChg = 01		120		
		BatReChg = 10		170		
		BatReChg = 11		220		
Maximum Precharge Time	t_{PCHG}	PChgTmr = 00		30		min
		PChgTmr = 01		60		
		PChgTmr = 10		120		
		PChgTmr = 11		240		
Maximum Fast Charge Time	t_{FCHG}	FChgTmr = 00		75		min
		FChgTmr = 01		150		
		FChgTmr = 10		300		
		FChgTmr = 11		600		
Charge Done Qualification	I_{CHG_DONE}	IChgDone = 00		I_{FCHG} x 0.050		mA
		IChgDone = 01	I_{FCHG} x 0.085	I_{FCHG} x 0.100	I_{FCHG} x 0.115	
		IChgDone = 10		I_{FCHG} x 0.200		
		IChgDone = 11		I_{FCHG} x 0.300		

Electrical Characteristics (continued)

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Maintain Charge Time	t_{MTCHG}	MtChgTmr = 00		0		min
		MtChgTmr = 01		15		
		MtChgTmr = 10		30		
		MtChgTmr = 11		60		
Timer Accuracy	t_{CHG_ACC}		-10		+10	%
Fast Charge Current Timer Extend Threshold	I_{FCHG_TEXT}	See Figure 4		50		$\%I_{FCHG}$
Fast Charge Current Timer Suspend Threshold	I_{FCHG_TSUS}	See Figure 4		20		$\%I_{FCHG}$
Battery Regulation Voltage Reduction Due to Temperature	$V_{BAT\_REG\_JTA}$	Cool/Room/WarmBatReg = 00		V_{BAT_REG} - 150mV		V
		Cool/Room/WarmBatReg = 01		V_{BAT_REG} - 100mV		
		Cool/Room/WarmBatReg = 10		V_{BAT_REG} - 50mV		
		Cool/Room/WarmBatReg = 11		V_{BAT_REG}		
Fast Charge Current Reduction Due to Temperature	I_{FCHG_JTA}	Cool/Room/WarmIFChg = 000		I_{FCHG} x 0.20		mA
		Cool/Room/WarmIFChg = 001		I_{FCHG} x 0.30		
		Cool/Room/WarmIFChg = 010		I_{FCHG} x 0.40		
		Cool/Room/WarmIFChg = 011		I_{FCHG} x 0.50		
		Cool/Room/WarmIFChg = 100		I_{FCHG} x 0.60		
		Cool/Room/WarmIFChg = 101		I_{FCHG} x 0.70		
		Cool/Room/WarmIFChg = 110		I_{FCHG} x 0.80		
		Cool/Room/WarmIFChg = 111		I_{FCHG}		

Electrical Characteristics (continued)

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BAT UVLO Threshold	V_{BAT_UVLO}	Rising (valid only when CHGIN is present, when V_{BAT} < V_{BAT_UVLO} the BAT-SYS switch opens and BAT is connected to SYS through a diode)		1.95	2.05	2.15	V
BAT UVLO Threshold Hysteresis	$V_{BAT\_UVLO\_H}$				50		mV
THERMISTOR MONITOR AND NTC DETECTION							
THM Hot Threshold	V_{THM_HOT}	Device specific (see Table 3)	V_{THM} falling, JEITASet = 0.	21.53	23.53	25.53	%V_{CAP}
			V_{THM} falling, JEITASet = 1,	30.94	32.94	34.94	
THM Warm Threshold	V_{THM_WARM}	Device specific (see Table 3)	V_{THM} falling, JEITASet = 0	30.94	32.94	34.94	%V_{CAP}
			V_{THM} falling, JEITASet = 1	48.20	50.20	52.20	
THM Cool Threshold	V_{THM_COOL}	V_{THM} rising		62.31	64.31	66.31	%V_{CAP}
THM Cold Threshold	V_{THM_COLD}	V_{THM} rising		71.73	73.73	75.73	%V_{CAP}
THM Disable Threshold	V_{THM_DIS}	V_{THM} rising		90.94	92.94	94.94	%V_{CAP}
THM Threshold Hysteresis	V_{THM_H}				60		mV
THM Input Leakage	I_{LK_THM}	V_{THM} = 0V to 5.5V		-1		+1	µA
TPU Input Leakage	I_{LK_TPU}	V_{TPU} = 0V to 5.5V		-1		+1	µA
TPUEXT Input Leakage	I_{LK_TPUEXT}	V_{TPUEXT} = 0V to 5.5V		-1		+1	µA
TPUEXT-to-TPU Switch Resistance	R_{TPUEXT_TPU}	V_{TPUEXT} = [1.0V, V_{SYS}], 3mA through switch			3	10	Ω
CAP-to-TPU Switch Resistance	R_{CAP_TPU}	3mA through switch			3	10	Ω
THM One-Shot Measurement Time	t_{THM_MEAS}	THM automatically selected as IVMON multiplexer output		450	500		ms
IVMON MULTIPLEXER							
IVMON Multiplexer Output Ratio	$V_{IVMON\_DIV\_RT}$	No load on IVMON pin. Inputs: Charger Current, BAT, SYS, BK1OUT, BK2OUT, BK3OUT, L1OUT, L2OUT, L3OUT, BBOUT, THM, TPU	MONRatioCfg = 00		100.0		%
			MONRatioCfg = 01		50.0		
			MONRatioCfg = 10		33.3		
			MONRatioCfg = 11		25.0		

Electrical Characteristics (continued)

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IVMON Multiplexer Output Impedance	R_{IVMON_DIV}	10µA load on IVMON pin. Inputs: Charger Current, BAT, SYS, BK1OUT, BK2OUT, BK3OUT, L1OUT, L2OUT, L3OUT, BBOUT, THM, TPU	MONRatioCfg = 00		5.5		kΩ
		1µA load on IVMON pin. Inputs: Charger Current, BAT, SYS, BK1OUT, BK2OUT, BK3OUT, L1OUT, L2OUT, L3OUT, BBOUT, THM, TPU	MONRatioCfg = 01		31.0		
			MONRatioCfg = 10		28.0		
			MONRatioCfg = 11		24.0		
IVMON Input Leakage	I_{LK_IVMON}	IVMON multiplexer disabled, pulldown resistance disabled, V_{IVMON} = 0V to 5.5V		-1		+1	µA
IVMON Multiplexer Off-State Pulldown Resistance	$R_{IVMON\_OFF\_PD}$	IVMON multiplexer disabled, pulldown resistance enabled			59		kΩ
BUCK							
Input Voltage Range	V_{IN}	Input voltage = V_{SYS}		2.700		5.500	V
Output Voltage Range	V_{BK_OUT}	10mV step resolution		0.700		1.330	V
		25mV step resolution		0.700		2.275	
		50mV step resolution		0.700		3.850	
Output Voltage UVLO	$V_{UVLO\_BK\_}$	Falling edge, hysteresis = 75mV		0.15	0.38	0.58	V

Electrical Characteristics (continued)

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Supply Current	$I_{Q\_BK\_}$	I_{BK_OUT} = 0, V_{SYS} = 3.7V (Note 3)	V_{BK_OUT} = 0.9V, 10mV step resolution		0.80	1.30	µA
			V_{BK_OUT} = 1.2V, 25mV step resolution		0.83	1.30	
			V_{BK_OUT} = 1.8V, 50mV step resolution		0.90	1.35	
Quiescent Supply Current in Dropout	$I_{Q\_DO\_BK\_}$	I_{BK_OUT} = 0, V_{SYS} - V_{BK_OUT} ≤ 0.1V			300		µA
Shutdown Supply Current with Active Discharge Enabled	$I_{SD\_BK\_}$	Buck_ disabled, Buck_ActDsc = 1			60		µA
Output Average Voltage Accuracy	ACC_BK_	I_{BK_OUT} = 1mA		-2.5		+2.5	%
Peak-to-Peak Voltage Ripple	$V_{RPP\_BK\_}$	Buck_ISet = 0100 (100mA), $C_{BK\_OUT\_EFF}$ = 2.2µF, I_{BK_OUT} = 1mA			10		mV
Peak Current Set Range	$I_{PSET\_BK\_}$	25mA step resolution. The accuracy of codes below 75mA is limited by $t_{ON\_MIN\_BK\_}$		0		375	mA
Load Regulation Error	LOAD_REG_BK_	Buck_ISet = 0110 (150mA), Buck_IAdptEn = 1, I_{BK_OUT} = 300mA			-3		%
Line Regulation Error	$V_{LINE\_REG\_BK\_}$	V_{SYS} from 2.7 to 5.5V			2		mV
Maximum Operative Output Current	I_{BK_MAX}	V_{SYS} = 3.7V, Buck_ISet = 1000 (200mA), Buck_IAdptEn = 1, load regulation error = -5%		220			mA
BK_OUT Pulldown Current with Buck Enabled	$I_{PD\_BK\_E}$	Buck_ enabled	10mV step resolution		40	100	nA
			25mV step resolution		100	200	
			50mV step resolution		200	400	
BK_OUT Pulldown Resistance with Buck Disabled	$R_{PD\_BK\_D}$	Buck_ disabled			17.5		MΩ
PMOS On-Resistance	$R_{P\_ON\_BK\_}$	Buck_FETScale = 0			0.35	0.49	Ω
	$R_{P\_ON\_BK\_FS}$	Buck_FETScale = 1			0.70	0.98	

Electrical Characteristics (continued)

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
NMOS On-Resistance	$R_{N\_ON\_BK\_}$	Buck_FETScale = 0			0.25	0.40	Ω
	$R_{N\_ON\_BK\_FS}$	Buck_FETScale = 1			0.50	0.70	
Freewheeling On-Resistance	$R_{ON\_BK\_FRWHL}$	V_{SYS} = 3.7V			7.5	12.5	Ω
Minimum On-Time	$t_{ON\_MIN\_BK\_}$				60	90	ns
Maximum Duty Cycle	D_MAX_BK_	Buck_IAdptEn = 1			95		%
Switching Frequency	FREQ_BK_	Load Regulation Error = -5%			3		MHz
Average Current During Short-Circuit to GND	$I_{SHRT\_BK\_}$	Buck_ISet = 0110 (150mA), Buck_IAdptEn = 1, V_{BK_OUT} = 0V			100		mA
BK_LX Leakage Current	$I_{LK\_BK\_LX}$	Buck_ disabled				1	µA
Active Discharge Current	$I_{ACTD\_BK\_}$			5	18	50	mA
Passive Discharge Resistance	$R_{PSV\_BK\_}$				10		kΩ
Full Turn-On Time	$t_{ON\_BK\_}$	Time from enable to full current capability, Buck_SftStrt = 1			58		ms
Efficiency	EFFIC_BK_	I_{BK_OUT} = 10mA, Inductor: Murata DFE201610E-2R2M	Buck_VSet = 0.9V, 10mV step resolution, Buck_ISet = 0111 (175mA)		87		%
			Buck_VSet = 1.2V, 25mV step resolution, Buck_ISet = 1000 (200mA)		89		
			Buck_VSet = 1.8V, 50mV step resolution, Buck_ISet = 1001 (225mA)		92		
BK_LX Rising/Falling Slew Rate	SLW_BK_	Buck_LowEMI = 0			2.0		V/ns
	SLW_BK_L	Buck_LowEMI = 1			0.5		
Thermal Shutdown Threshold	$T_{SHDN\_BK\_}$				140		°C

Electrical Characteristics (continued)

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LDO1 (ALWAYS ON LDO OPTION)						
Input Voltage	V_{L1IN}	LDO mode	2.7		5.5	V
		Switch mode	1.2		5.5	
Quiescent Supply Current	I_{Q_L1}	LDO enabled, I_{L1OUT} = 0µA, V_{L1IN} = 3.7V, LDO1VSet = 3.0V (Note 3)		0.50	1.10	µA
		LDO enabled, I_{L1OUT} = 0µA, switch mode, V_{L1IN} = 3.7V (Note 3)		0.32	0.55	
Quiescent Supply Current in Dropout	$I_{Q\_L1\_DRP}$	I_{L1OUT} = 0µA, V_{L1IN} = 2.9V, LDO1VSet = 3.0V (Note 3)		88	120	µA
Shutdown Supply Current with Active Discharge Enabled	I_{SD_L1}	LDO disabled, LDO1ActDsc = 1		55		µA
Output Leakage	I_{LK_L1OUT}	V_{L1OUT} = GND, LDO disabled			1	µA
Maximum Output Current	I_{L1OUT_MAX}		100			mA
Output Voltage Range	V_{L1OUT}	100mV step resolution	0.8		3.6	V
Output Voltage Accuracy	ACC_LDO1	V_{L1IN} = (V_{L1OUT} + 0.5V) or higher, I_{L1OUT} = 1mA	-2.7		+2.7	%
Dropout Voltage	V_{DRP_L1}	V_{L1IN} = 2.9V, I_{L1OUT} = 100mA, LDO1VSet = 3.0V			95	mV
Line Regulation Error	$V_{LINE\_REG\_L1}$	V_{L1IN} = (V_{L1OUT} + 0.5V) to 5.5V, I_{L1OUT} = 1mA	-0.12		+0.12	%/V
Load Regulation Error	$V_{LOAD\_REG\_L1}$	I_{L1OUT} = 100µA to 100mA		0.002	0.005	%/mA
Line Transient	$V_{LINE\_TRAN\_L1}$	V_{L1IN} = 4V to 5V, 200ns rise time		±36		mV
		V_{L1IN} = 4V to 5V, 1µs rise time		±28		
Load Transient	$V_{LOAD\_TRAN\_L1}$	I_{L1OUT} = 0mA to 10mA, 200ns rise time		130		mV
		I_{L1OUT} = 0mA to 100mA, 200ns rise time		290		
Passive Discharge Resistance	R_{PSV_L1}		4	10	17	kΩ
Active Discharge Current	I_{ACTD_L1}	V_{L1IN} = 3.7V	7	20	36	mA
Switch Mode Resistance	R_{ON_L1}	V_{L1IN} = 1.8V, I_{L1OUT} = 100mA		0.63	1.00	Ω
		V_{L1IN} = 1.2V, I_{L1OUT} = 5mA		1.40	2.30	
Turn-On Time	t_{ON_L1}	I_{L1OUT} = 0mA, time from 10% to 90% of final value		1.60		ms
		I_{L1OUT} = 0mA, time from 10% to 90% of final value, switch mode		0.25		
Short-Circuit Current Limit	I_{SHRT_L1}	V_{L1IN} = 2.7V, V_{L1OUT} = 0V	220	400	590	mA
Thermal Shutdown Temperature	T_{SHDN_L1}			150		°C

Electrical Characteristics (continued)

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Thermal Shutdown Temperature Hysteresis	$T_{SHDN\_HYS\_L1}$				20		°C
Output Noise	V_{NOISE_L1}	10Hz to 100kHz, V_{L1IN} = 5V	LDO1VSet = 3.3V		110		μV_{RMS}
			LDO1VSet = 2.5V		95		
			LDO1VSet = 1.2V		60		
			LDO1VSet = 0.8V		60		
LDO2							
Input Voltage	V_{L2IN}	LDO mode		1.71		5.50	V
		Switch mode		1.20		5.50	
Quiescent Supply Current	I_{Q_L2}	LDO enabled, I_{L2OUT} = 0µA (Note 3)			1.00	2.00	µA
		LDO enabled, I_{L2OUT} = 0µA, switch mode (Note 3)			0.32	0.60	
Quiescent Supply Current in Dropout	$I_{Q\_L2\_DRP}$	I_{L2OUT} = 0µA, V_{L2IN} = 2.9V, LDO2VSet = 3.0V			2.0	3.8	µA
Shutdown Supply Current with Active Discharge Enabled	I_{SD_L2}	LDO disabled, LDO2ActDsc = 1			50		µA
Output Leakage	I_{LK_L2OUT}	V_{L2OUT} = GND, LDO disabled				1	µA
Maximum Output Current	I_{L2OUT_MAX}	V_{L2IN} > 1.8V		100			mA
		V_{L2IN} ≤ 1.8V		50			
Output Voltage Range	V_{L2OUT}	100mV step resolution		0.9		4.0	V
Output Voltage Accuracy	ACC_LDO2	V_{L2IN} = (V_{L2OUT} + 0.5V) or higher, I_{L2OUT} = 1mA		-2.7		+2.7	%
Dropout Voltage	V_{DRP_L2}	V_{L2IN} = 2.9V, I_{L2OUT} = 100mA, LDO2VSet = 3V				90	mV
Line Regulation Error	$V_{LINE\_REG\_L2}$	V_{L2IN} = (V_{L2OUT} + 0.5V) to 5.5V, I_{L2OUT} = 1mA		-0.45		+0.45	%/V
Load Regulation Error	$V_{LOAD\_REG\_L2}$	I_{L2OUT} = 100µA to 100mA			0.001	0.007	%/mA
Line Transient	$V_{LINE\_TRAN\_L2}$	V_{L2IN} = 4V to 5V, 200ns rise time			±35		mV
		V_{L2IN} = 4V to 5V, 1µs rise time			±25		
Load Transient	$V_{LOAD\_TRAN\_L2}$	I_{L2OUT} = 0mA to 10mA, 200ns rise time			100		mV
		I_{L2OUT} = 0mA to 100mA, 200ns rise time			200		
Passive Discharge Resistance	R_{PSV_L2}			4	10	17	kΩ
Active Discharge Current	I_{ACTD_L2}	V_{L2IN} = 3.7V		7	20	36	mA
Switch Mode Resistance	R_{ON_L2}	V_{L2IN} = 1.8V, I_{L2OUT} = 100mA			0.60	0.97	Ω
		V_{L2IN} = 1.2V, I_{L2OUT} = 5mA			1.30	2.20	

Electrical Characteristics (continued)

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Turn-On Time	t_{ON_L2}	I_{L2OUT} = 0mA, time from 10% to 90% of final value			1.50		ms
		I_{L2OUT} = 0mA, time from 10% to 90% of final value, switch mode			0.25		
Short-Circuit Current Limit	I_{SHRT_L2}	V_{L2IN} = 2.7V, V_{L2OUT} = GND		220	400	590	mA
Thermal Shutdown Temperature	T_{SHDN_L2}				150		°C
Thermal Shutdown Temperature Hysteresis	$T_{SHDN\_HYS\_L2}$				20		°C
L2IN UVLO	V_{UVLO_L2}	V_{L2IN} falling		1.14	1.32		V
		V_{L2IN} rising			1.35	1.59	
Output Noise	V_{NOISE_L2}	10Hz to 100kHz, V_{L2IN} = 5V	LDO2VSet = 3.3V		110		μV_{RMS}
			LDO2VSet = 2.5V		95		
			LDO2VSet = 1.2V		60		
			LDO2VSet = 0.9V		60		
LDO3							
Input Voltage	V_{L3IN}	LDO mode		1.0		2.0	V
		Switch mode		0.7		2.0	
Quiescent Supply Current	I_{Q_L3}	LDO enabled, I_{L3OUT} = 0µA (Note 3)			1.05	2.65	µA
		LDO enabled, I_{L3OUT} = 0µA, switch mode (Note 3)			0.26	0.60	
		LDO enabled, I_{L3OUT} = 0µA, LDO3_MPC0CNT = 1, MPC0 high (Note 3)			0.70	1.35	
Quiescent Supply Current in Dropout	$I_{Q\_L3\_DRP}$	I_{L3OUT} = 0µA, V_{L3IN} = 1.2V, LDO3VSet = 1.3V (Note 3)			2.4	4.6	µA
Output Leakage	I_{LK_L3OUT}	V_{L3OUT} = GND, LDO disabled			0.015	2.500	µA
Shutdown Supply Current with Active Discharge Enabled	I_{SD_L3}	LDO disabled, LDO3ActDsc = 1			50		µA
Maximum Output Current	I_{L3OUT_MAX}			50			mA
Output Voltage Range	V_{L3OUT}	25mV step resolution		0.50		1.95	V
Output Voltage Accuracy	ACC_LDO3	V_{L3IN} = (V_{L3OUT} + 0.2V) or higher, I_{L3OUT} = 1mA		-3		+3	%
Dropout Voltage	V_{DRP_L3}	V_{L3IN} = 1V, I_{L3OUT} = 50mA, LDO3VSet = 1.025V				75	mV
Line Regulation Error	$V_{LINE\_REG\_L3}$	V_{L3IN} = (V_{L3OUT} + 0.2V) to 2V, I_{L3OUT} = 1mA		-0.4		+0.4	%/V
Load Regulation Error	$V_{LOAD\_REG\_L3}$	I_{L3OUT} = 100µA to 50mA			0.003	0.013	%/mA

Electrical Characteristics (continued)

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Line Transient	$V_{LINE\_TRAN\_L3}$	V_{L3IN} = 1V to 2V, 200ns rise time			±45		mV
		V_{L3IN} = 1V to 2V, 1µs rise time			±25		
Load Transient	$V_{LOAD\_TRAN\_L3}$	I_{L3OUT} = 0mA to 10mA, 200ns rise time			80		mV
		I_{L3OUT} = 0mA to 50mA, 200ns rise time			130		
Passive Discharge Resistance	R_{PSV_L3}			4	10	17	kΩ
Active Discharge Current	I_{ACTD_L3}	V_{L3IN} = 1.8V		10	30	60	mA
Switch Mode Resistance	R_{ON_L3}	V_{L3IN} = 1.8V, I_{L3OUT} = 50mA			0.40	0.64	Ω
		V_{L3IN} = 0.7V, I_{L3OUT} = 1mA			1.50	3.30	
Turn-On Time	t_{ON_L3}	I_{L3OUT} = 0mA, time from 10% to 90% of final value			380		µs
		I_{L3OUT} = 0mA, time from 10% to 90% of final value, switch mode			65		
		I_{L3OUT} = 0mA, LDO3_MPC0CNT = 1, time from MPC0 rising to 90% of L3OUT final value, C_{L3OUT} = 10nF			155	350	ns
Short-Circuit Current Limit	I_{SHRT_L3}	V_{L3IN} = 1.2V, V_{L3OUT} = GND			345	950	mA
		V_{L3IN} = 1.2V, V_{L3OUT} = GND, switch mode			310	700	
Thermal Shutdown Temperature	T_{SHDN_L3}				150		°C
Thermal Shutdown Temperature Hysteresis	$T_{SHDN\_HYS\_L3}$				20		°C
L3IN UVLO	V_{UVLO_L3}	V_{L3IN} falling		0.65	0.77		V
		V_{L3IN} rising			0.78	0.95	
Output Noise	V_{NOISE_L3}	10Hz to 100kHz, V_{L3IN} = 2V	LDO3VSet = 1.8V		120		$µV_{RMS}$
			LDO3VSet = 1.0V		95		
			LDO3VSet = 0.5V		70		
BUCK-BOOST							
Input Voltage Range	V_{BBIN}	Input voltage = V_{SYS}		2.7		5.5	V
Output Voltage Range	V_{BBOUT}	50mV step resolution, do not exceed the valid voltage range.		2.6		5.5	V
Quiescent Supply Current	I_{Q_BB}	I_{BBOUT} = 0µA, V_{BBOUT} = 5V (Note 3)			2.5	5.0	µA
Shutdown Supply Current with Active Discharge Enabled	I_{SD_BB}	Buck-Boost disabled, BBstActDsc = 1			60		µA

Electrical Characteristics (continued)

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Output Operative Power	P_{MAX_BBOUT}	BBstIpPadPEnb = 0, V_{BBIN} ≥ 3.2V, V_{BBOUT} ≥ 3.2V at 7.5% load regulation (Note 3)	1.5			W
Load Regulation Error	LOAD_REG_ERR	BBstIpPadPEnb= 0, BBstVSet > 3.3V, P_{OUT} = 1.5W		-3.5		%
Average Output Voltage Accuracy	ACC_BBOUT	I_{BBOUT} = 1mA, C_{BBOUT_EFF} ≥ 5µF	-3		+3	%
Maximum Output Current During Startup	$I_{LOAD\_MAX\_STUP}$	V_{BBIN} > 3V, BBstIpPadPEnb = 0	100			mA
Startup time	t_{STUP}	I_{LOAD} < $I_{LOAD\_MAX\_STUP}$, time from V_{BBOUT} = 0V to final value		13		ms
Input Supply Current During Startup	I_{BBIN_STUP}	V_{BBIN} = 3.6V, V_{BBOUT} = 5V, C_{BBOUT_EFF} = 10µF, I_{BBOUT} = 0		10		mA
Output UVLO Threshold	V_{BBOUT_UVLO}	Falling edge (50mV hysteresis)		1.85	2.46	V
HVLX Leakage Current	I_{LK_BBH} VLX				1	µA
LVLX Leakage Current	I_{LK_BBL} VLX				1	µA
Passive Discharge Resistance	R_{PSV_BB}		5	10	17	kΩ
Active Discharge Current	I_{ACTD_BB}	V_{BBOUT} = 2.5V	5	20	50	mA
BBOUT Pulldown Current	$I_{PD\_BB\_E}$	BB enabled		200		nA
Thermal Shutdown Threshold	T_{SHDN_BB}			150		°C
LOAD SWITCHES (TYPICAL VALUES AT V_{LSW_IN} = 1.2V)						
Input Voltage	V_{LSW_IN}		0.65		5.50	V
Quiescent Supply Current	$I_{Q\_LSW\_}$	Load switch on, voltage protection enabled, V_{LSW_IN} = 1.2V (Note 3)		0.80	1.20	µA
		Load switch on, voltage protection disabled, V_{LSW_IN} = 1.2V (Note 3)		0.26	0.45	
On-Resistance	$R_{ON\_LSW\_}$	V_{SYS} = 3V, V_{LSW_IN} = 1.2V, I_{LSW_OUT} = 50mA		0.44	0.75	Ω
Startup Current	I_{LSW_START}	V_{LSW_IN} = 1.2V, V_{LSW_OUT} = 0V initially	22	63	108	mA
Voltage Protection Threshold	V_{LSW_PROT}	Rising		130	250	mV
		Falling	4	120		
Turn-On Time	$t_{ON\_LSW\_}$	V_{LSW_IN} = 1.2V, 1µF output capacitance, from 10% to 90% of final value		15		µs
Startup Time-Out Time	t_{STUP_LSW}			5		ms

Electrical Characteristics (continued)

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Startup Retry Time	$t_{RETRY\_LSW\_}$			5		ms
Passive Discharge Resistance	$R_{PSV\_LSW\_}$		4	10	17	kΩ
Active Discharge Current	$I_{ACTD\_LSW\_}$		7	20	36	mA
Output Leakage	$I_{LK\_LSW\_}$	LSW_OUT = GND, load switch disabled			1	µA
DIGITAL						
SDA, SCL, MPC_, PFN_, $\overline{RST}$, $\overline{INT}$ Input Leakage Current	I_{LK_IO}	Input pullup/pulldown resistances disabled, V_{IO} = 0V to 5.5V	-1		+1	µA
SDA, SCL, MPC_ Input Logic High	V_{IO_IH}		1.4			V
SDA, SCL, MPC_ Input Logic Low	V_{IO_IL}				0.4	V
PFN_ Input Logic High	$V_{PFN\_IH\_C}$	Off mode	0.7 x V_{VCCINT}			V
PFN_ Input Logic Low	$V_{PFN\_IL\_C}$	Off mode		0.3 x V_{VCCINT}		V
PFN_ Input Logic High	$V_{PFN\_IH\_T}$	On mode	1.4			V
PFN_ Input Logic Low	$V_{PFN\_IL\_T}$	On mode			0.4	V
MPC_, PFN_ Input Pullup Resistance	R_{IO_PU}	Pullup resistance to VCCINT (Note 2)		170		kΩ
MPC_, PFN_ Input Pulldown Resistance	R_{IO_PD}			170		kΩ
MPC_ Output Logic-High	V_{IO_OH}	I_{OH} = 1mA, MPC_ configured as push-pull output, pullup voltage is V_{BK3OUT}	V_{BK3OUT} - 0.4			V
SDA, $\overline{RST}$, $\overline{INT}$, MPC_, PFN_ Output Logic Low	V_{IO_OL}	I_{OL} = 4mA			0.4	V
SCL Clock Frequency	f_{SCL}		0		1000	kHz
Bus Free Time Between STOP and START Condition	t_{BUF}		0.5			µs
START Condition (Repeated) Hold Time	t_{HD_STA}		0.26			µs
Low Period of SCL Clock	t_{LOW}		0.5			µs
High Period of SCL Clock	t_{HIGH}		0.26			µs
Setup Time for a Repeated START Condition	t_{SU_STA}		0.26			µs
Data Hold Time	t_{HD_DAT}		0.0		0.9	µs
Data Setup Time	t_{SU_DAT}		50			ns

Electrical Characteristics (continued)

(V_{BAT} = V_{SYS_UVLO} (falling) to +5.5V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to +28V. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 8.8µF, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH. Limits are 100% tested at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}		50			ns
SPI						
SCLK Frequency	f_{SCLK}	(Note 3)			10	MHz
$\overline{CS}$ Setup Time	t_{CS}		10			ns
$\overline{CS}$ Hold Time	t_{CH}		100			ns
$\overline{CS}$ Pulse-Width High	t_{IDLE}			60		ns
DIN Setup Time	t_{DS}		10			ns
DIN Hold Time	t_{DH}		20			ns
SCLK Pulse-Width Low	t_{LOW_SPI}		20			ns
SCLK Pulse-Width High	t_{HIGH_SPI}		20			ns

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

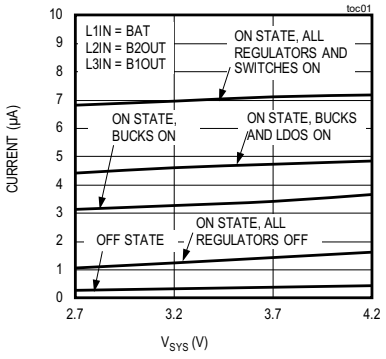
Note 2: V_{VCCINT} is an internal voltage supply generated from either V_{BAT} or V_{CAP}. The source is determined by the following:if [(V_{CHGIN} > V_{CHGIN_DET} AND V_{CAP} > V_{CAP_DET}) or V_{CAP} > (V_{BAT} + $V_{THSWOVER}$)], then V_{VCCINT} = V_{CAP}, ELSE V_{VCCINT} = V_{BAT} where $V_{THSWOVER}$ = [0-300]mV

Note 3: Quiescent current is guaranteed by design only and not production tested.

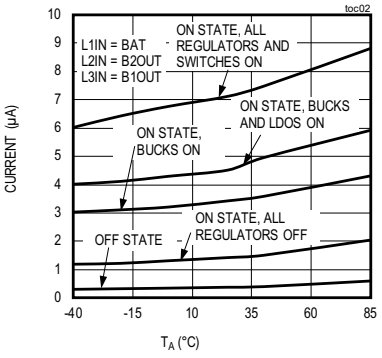
Typical Operating Characteristics

(V_{BAT} = +3.7V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 4.4µF, V_{BBOUT} = 5V, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25°C, unless otherwise noted.)

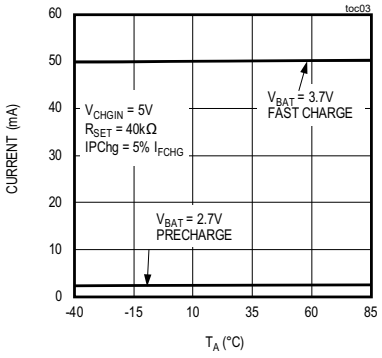
BAT INPUT CURRENT vs. SYS VOLTAGE



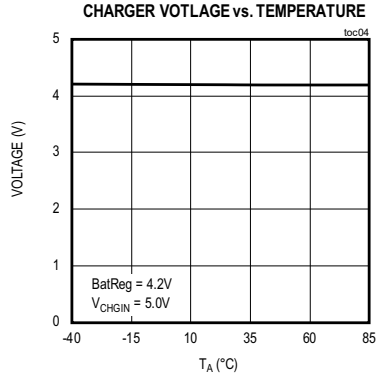
BAT INPUT CURRENT vs. TEMPERATURE



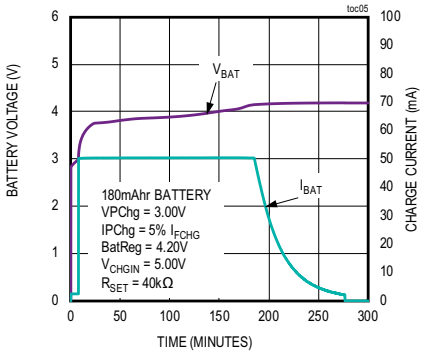
CHARGER CURRENT vs. TEMPERATURE



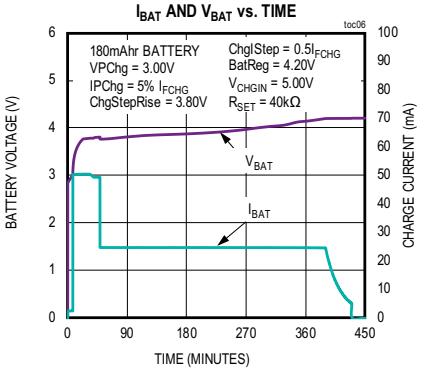
CHARGER VOTLAGE vs. TEMPERATURE



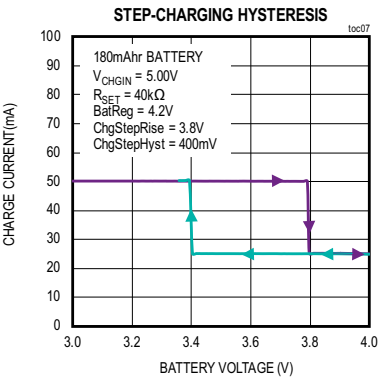
CHARGER PROFILE
IBAT AND VBAT vs. TIME



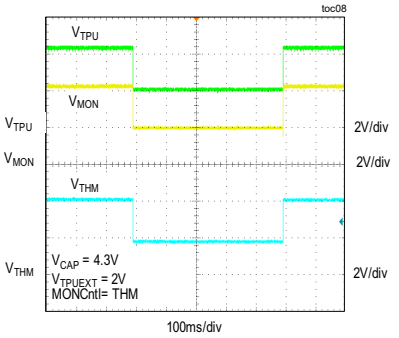
STEP-CHARGING CHARGER PROFILE
IBAT AND VBAT vs. TIME



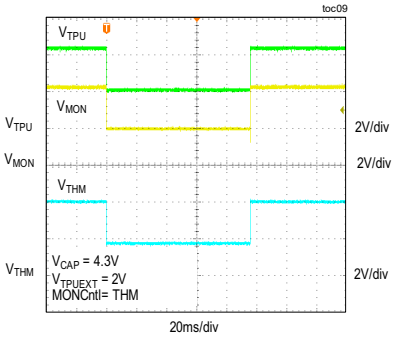
STEP-CHARGING HYSTERESIS



THM ONE-SHOT MEASUREMENT



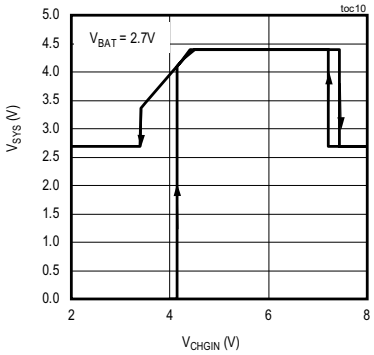
THM ONE-SHOT MEASUREMENT ABORT



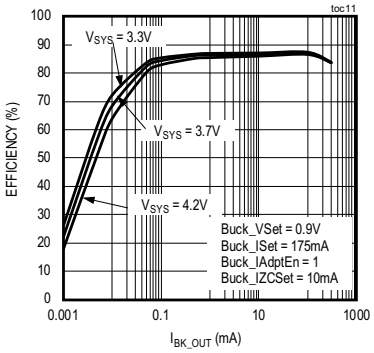
Typical Operating Characteristics (continued)

(V_{BAT} = +3.7V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 4.4µF, V_{BBOUT} = 5V, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25°C, unless otherwise noted.)

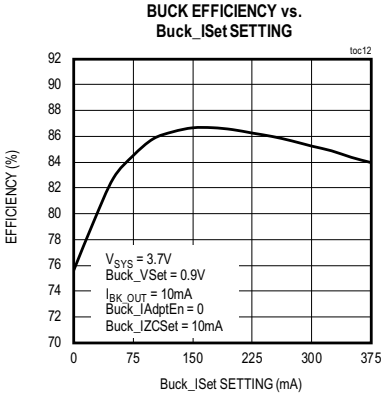
SYS VOLTAGE vs. CHGIN VOLTAGE



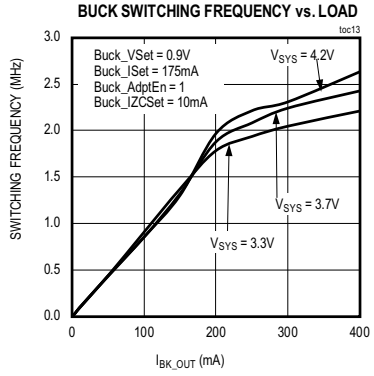
BUCK EFFICIENCY vs. LOAD



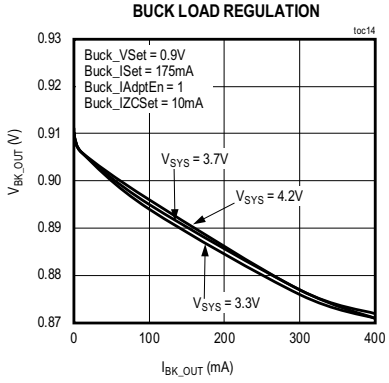
BUCK EFFICIENCY vs. Buck_ISet SETTING



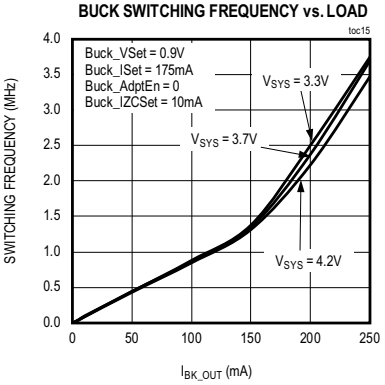
BUCK SWITCHING FREQUENCY vs. LOAD



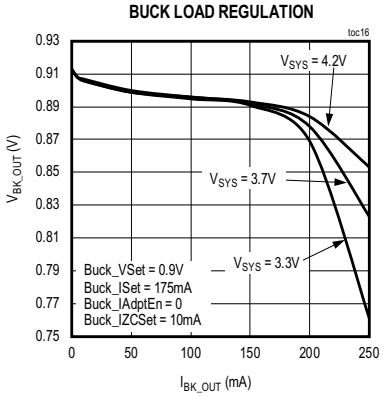
BUCK LOAD REGULATION



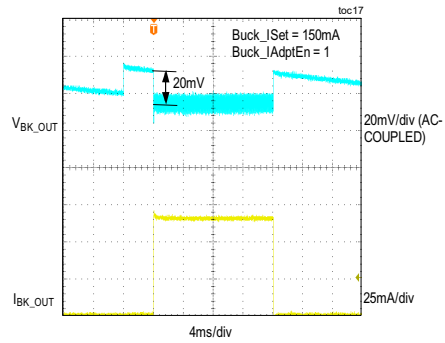
BUCK SWITCHING FREQUENCY vs. LOAD



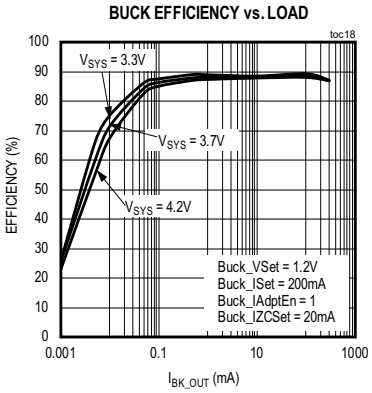
BUCK LOAD REGULATION



BUCK LOAD TRANSIENT



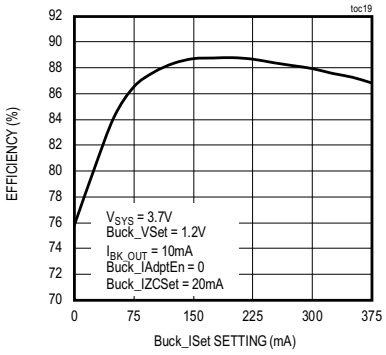
BUCK EFFICIENCY vs. LOAD



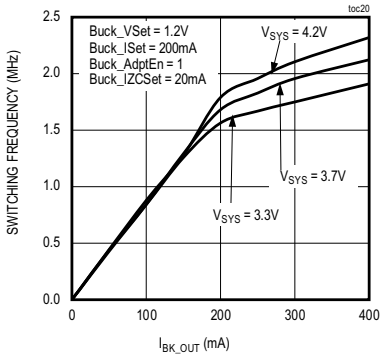
Typical Operating Characteristics (continued)

(V_{BAT} = +3.7V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 4.4µF, V_{BBOUT} = 5V, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25°C, unless otherwise noted.)

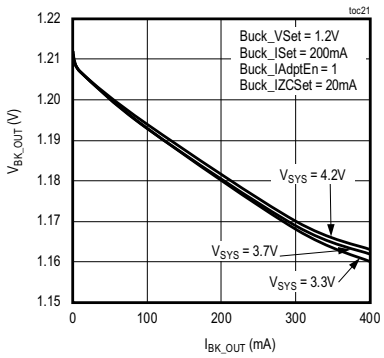
BUCK EFFICIENCY vs. Buck_ISet SETTING



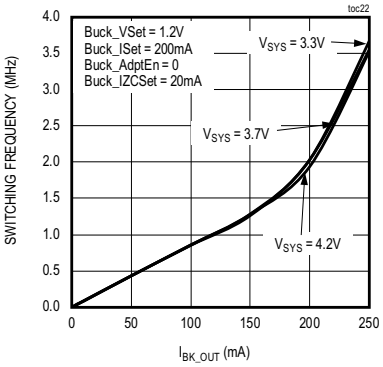
BUCK SWITCHING FREQUENCY vs. LOAD



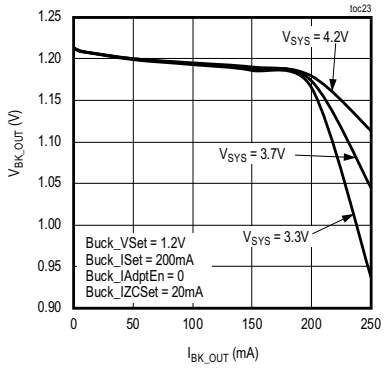
BUCK LOAD REGULATION



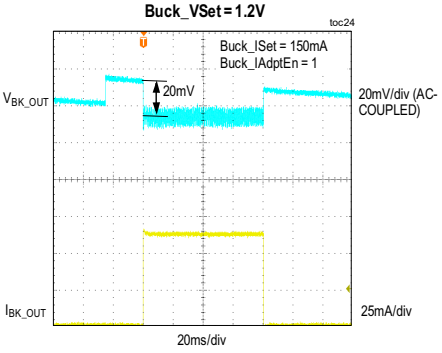
BUCK SWITCHING FREQUENCY vs. LOAD



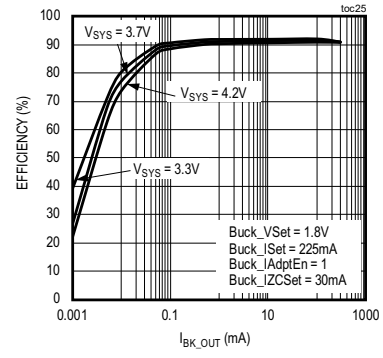
BUCK LOAD REGULATION



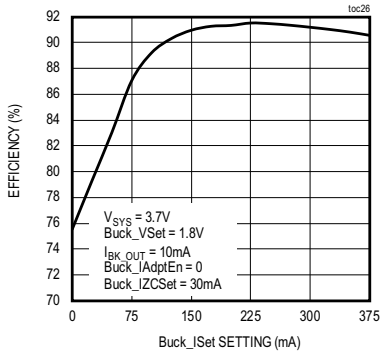
BUCK LOAD TRANSIENT Buck_VSet = 1.2V



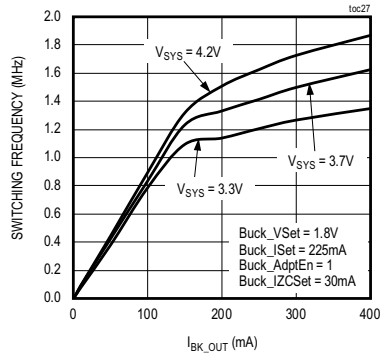
BUCK EFFICIENCY vs. LOAD



BUCK EFFICIENCY vs. Buck_ISet SETTING



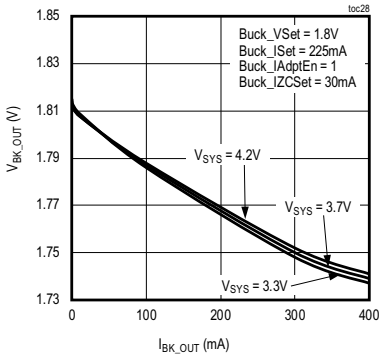
BUCK SWITCHING FREQUENCY vs. LOAD



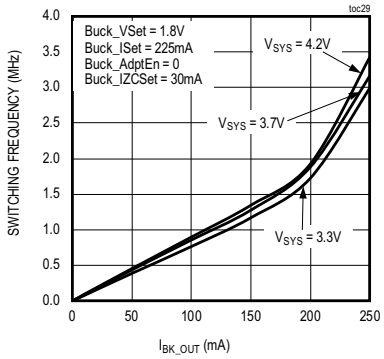
Typical Operating Characteristics (continued)

(V_{BAT} = +3.7V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 4.4µF, V_{BBOUT} = 5V, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25°C, unless otherwise noted.)

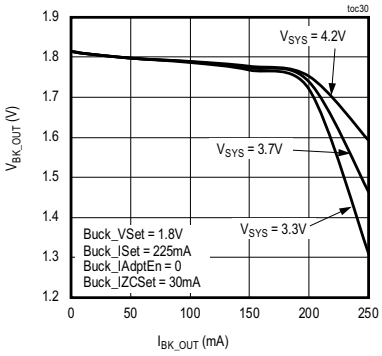
BUCK LOAD REGULATION



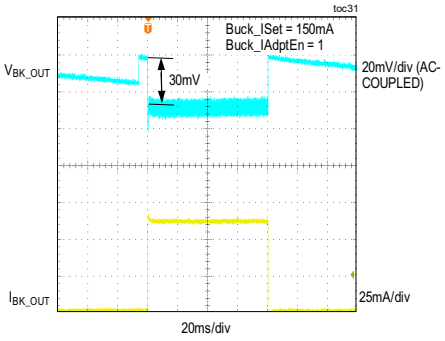
BUCK SWITCHING FREQUENCY vs. LOAD



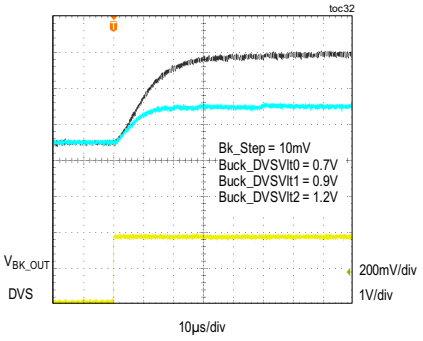
BUCK LOAD REGULATION



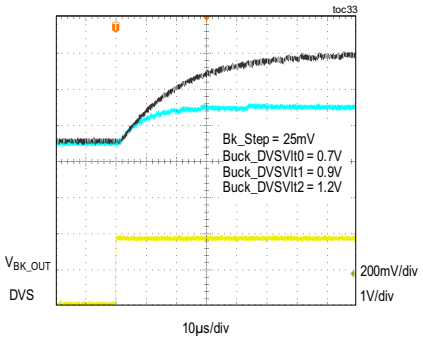
BUCK LOAD TRANSIENT
Buck_VSet = 1.8V



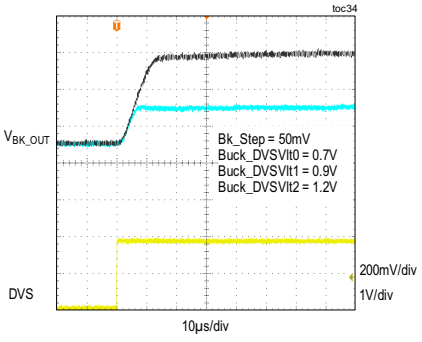
BUCK DVS MODE 1 TRANSITION
Bk_Step = 10mV



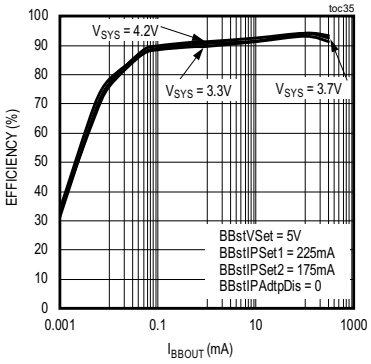
BUCK DVS MODE 1 TRANSITION
Bk_Step = 25mV



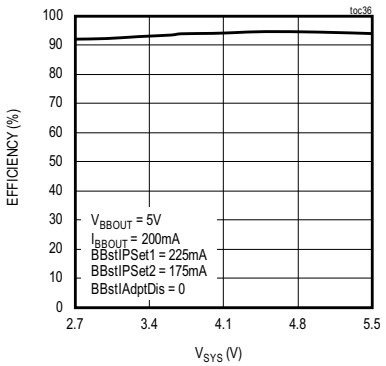
BUCK DVS MODE 1 TRANSITION
Bk_Step = 50mV



BUCK-BOOST EFFICIENCY vs. LOAD BUCK-BOOST MODE



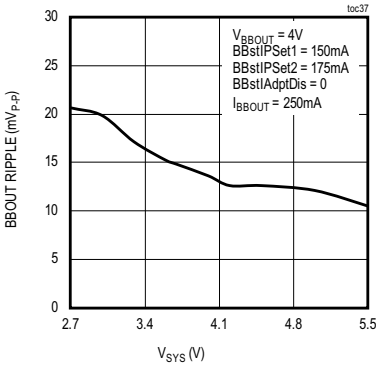
BUCK-BOOST EFFICIENCY vs. SYS VOLTAGE



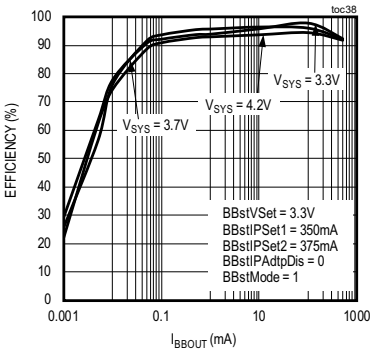
Typical Operating Characteristics (continued)

(V_{BAT} = +3.7V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 4.4µF, V_{BBOUT} = 5V, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25°C, unless otherwise noted.)

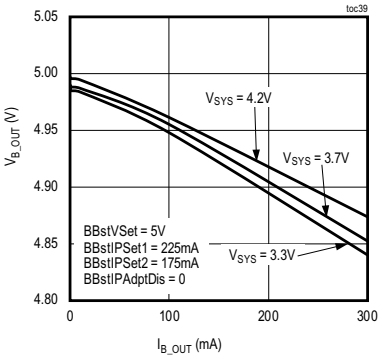
BUCK-BOOST RIPPLE vs. SYS VOLTAGE



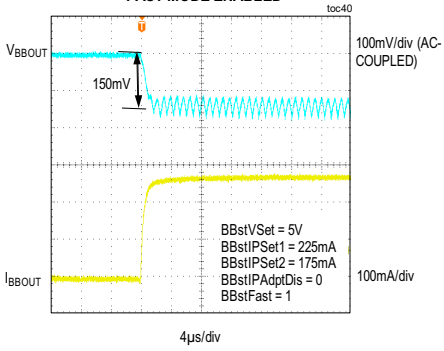
BUCK-BOOST EFFICIENCY vs. LOAD BUCK-ONLY MODE



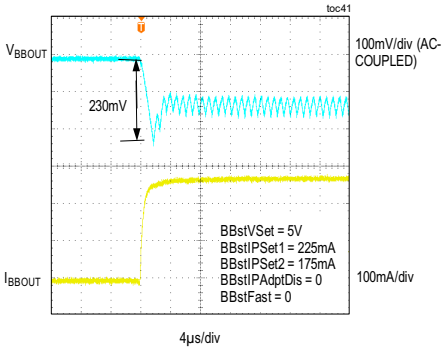
BUCK-BOOST LOAD REGULATION



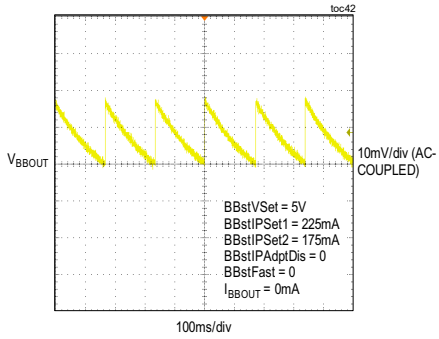
BUCK-BOOST LOAD TRANSIENT FAST MODE ENABLED



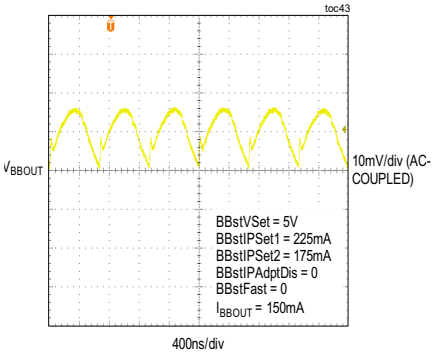
BUCK-BOOST LOAD TRANSIENT FAST MODE DISABLED



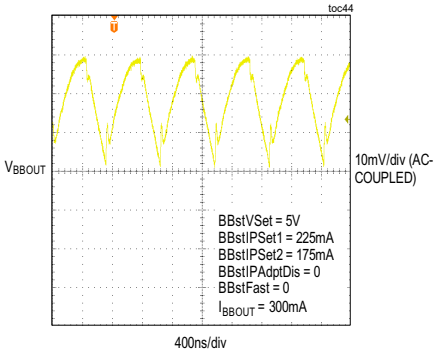
BUCK-BOOST RIPPLE NO LOAD



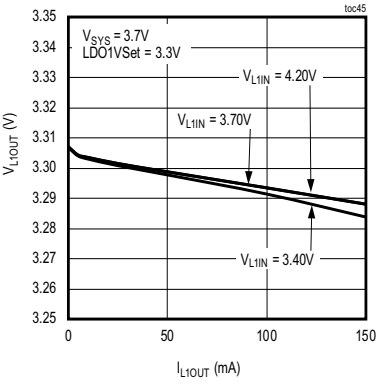
BUCK-BOOST RIPPLE MODERATE LOAD



BUCK-BOOST RIPPLE HEAVY LOAD



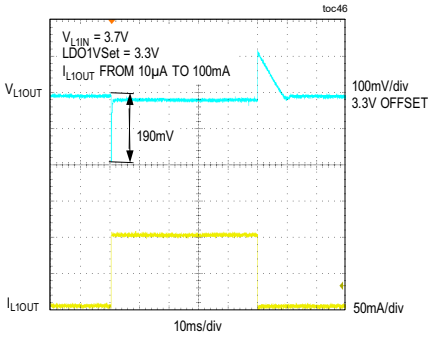
LDO1 LOAD REGULATION



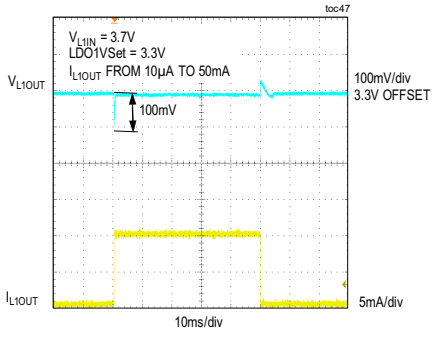
Typical Operating Characteristics (continued)

(V_{BAT} = +3.7V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 4.4µF, V_{BBOUT} = 5V, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25°C, unless otherwise noted.)

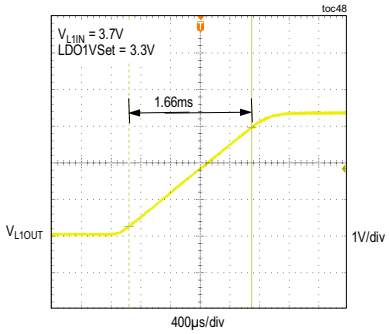
LDO1 LOAD TRANSIENT



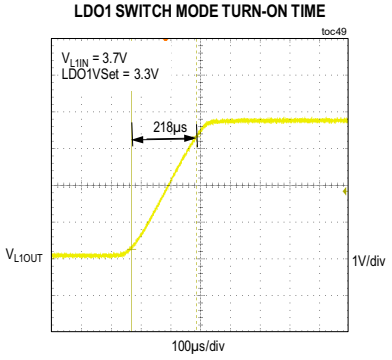
LDO1 LOAD TRANSIENT 10µA - 10mA



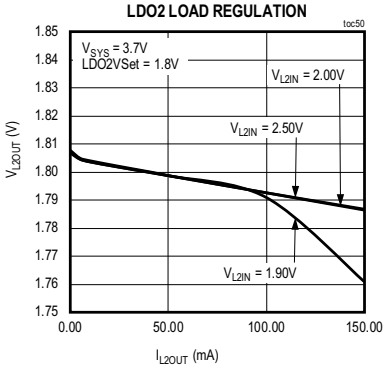
LDO1 LDO MODE TURN-ON TIME



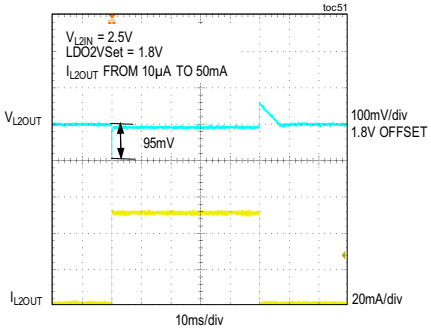
LDO1 SWITCH MODE TURN-ON TIME



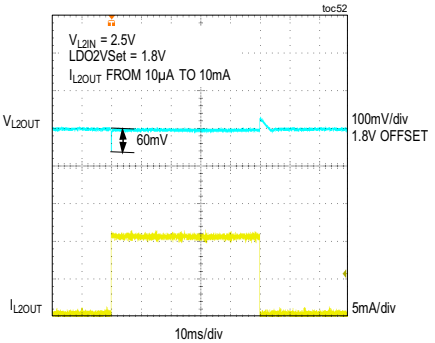
LDO2 LOAD REGULATION



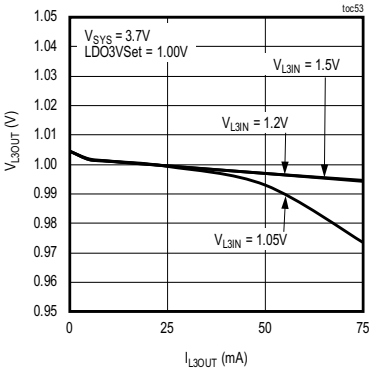
LDO2 LOAD TRANSIENT 10µA - 50mA



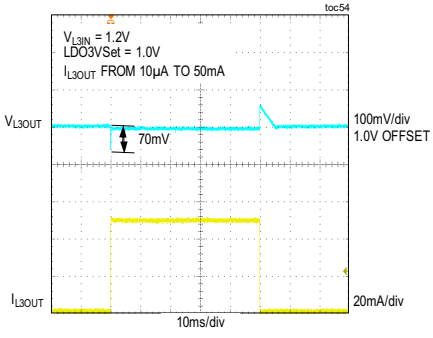
LDO2 LOAD TRANSIENT 10µA - 10mA



LDO3 LOAD REGULATION



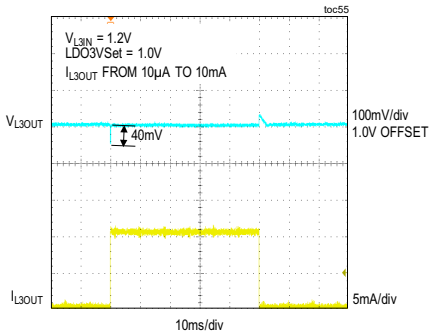
LDO3 LOAD TRANSIENT 10µA - 50mA



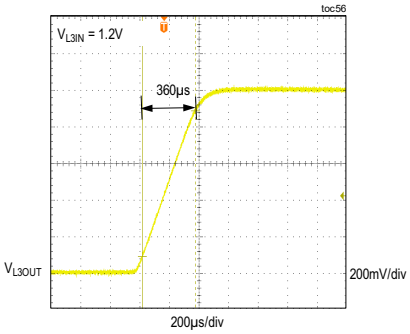
Typical Operating Characteristics (continued)

(V_{BAT} = +3.7V, C_{CHGIN} = 1µF, C_{CAP} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, $C_{BK\_OUT\_EFF}$ = 10µF, C_{L_IN} = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 4.4µF, V_{BBOUT} = 5V, $L_{BK\_}$ = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25°C, unless otherwise noted.)

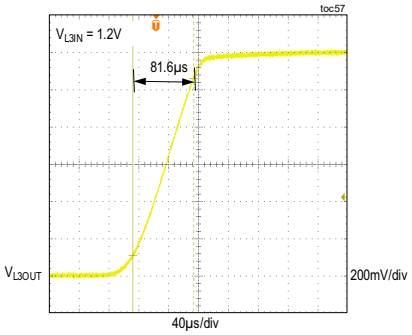
LDO3 LOAD TRANSIENT
10µA - 10mA



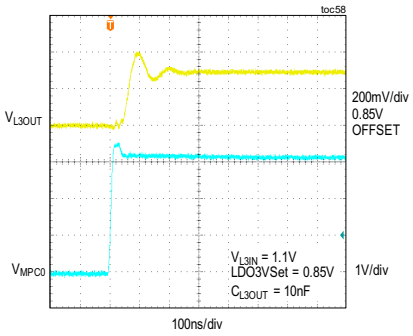
LDO3 LDO MODE TURN-ON TIME



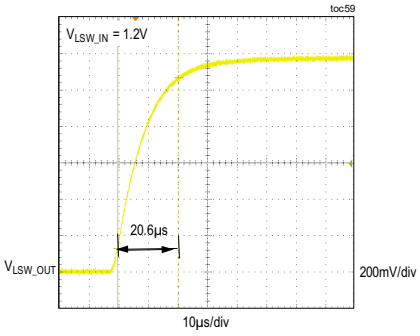
LDO3 SWITCH MODE TURN-ON TIME



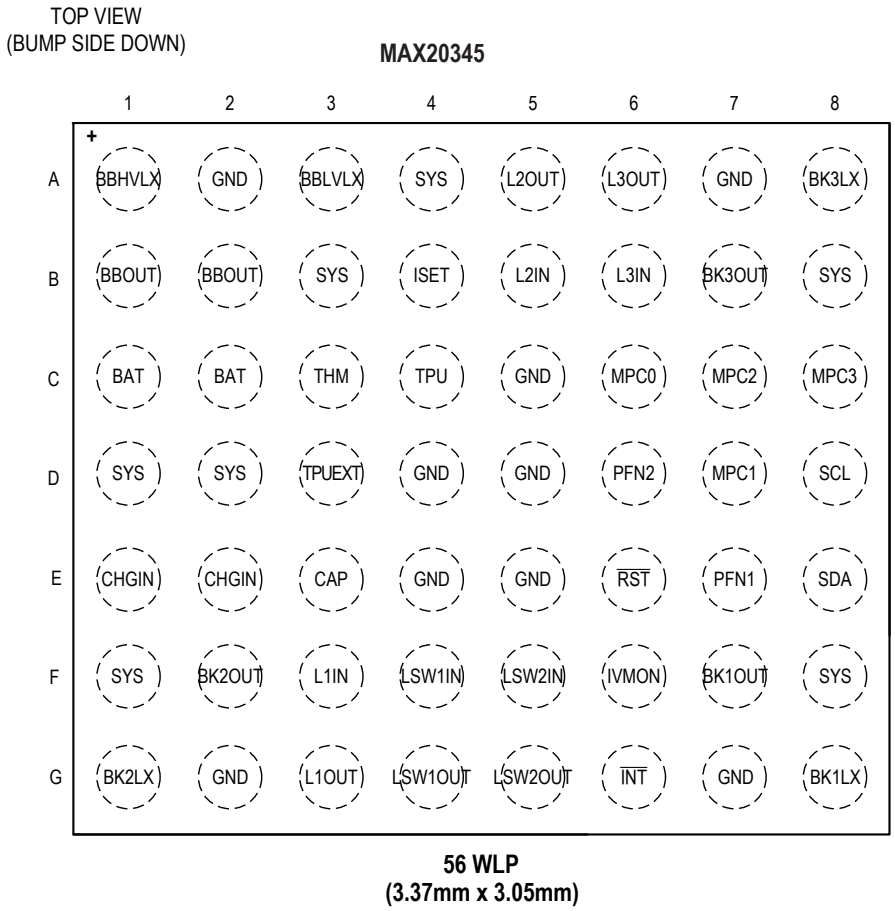
LDO3 LDO MODE TO SWITCH MODE
MPC0 CONTROL



LOAD SWITCH TURN-ON TIME



Pin Configuration



56 WLP
(3.37mm x 3.05mm)

Pin Description

PIN	NAME	FUNCTION
A1	BBHVLX	Buck-Boost Regulator Switch HV Side. Connect through 2.2µH inductor to BBLVLX.
A2, A7, C5, D4, D5, E4, E5, G2, G7	GND	Ground. All GND bumps must be connected on PCB using a low-impedance trace or GND plane.
A3	BBLVLX	Buck-Boost Regulator Switch LV Side. Connect through 2.2µH inductor to BBHVLX.
A4, B3, B8, D1, D2, F1, F8	SYS	System Load Connection. All SYS bumps must be connected on PCB using a low-impedance trace or SYS plane. Bypass common node with a minimum 10µF of capacitance to GND.
A5	L2OUT	LDO2 Output. Bypass with 1µF of capacitance to GND.
A6	L3OUT	LDO3 Output. Bypass with 1µF of capacitance to GND.
A8	BK3LX	Buck3 Regulator Switch. Connect through 2.2µH to BK3OUT.
B1, B2	BBOUT	Buck-Boost Regulator Output. Bypass to GND with effective capacitance equal to the value of the derating curve (*Figure 5*) for a bias voltage V_{OUT}, placed as close to the device as possible..
B4	ISET	External Resistor for Battery Charge Current Level Setting. Do not connect any capacitance on this pin. Maximum allowed capacitance: $C_{ISET} < (5µs/R_{ISET})$ pF.
B5	L2IN	LDO2 Input. Bypass with 1µF capacitor to GND
B6	L3IN	LDO3 Input. Bypass with 1µF capacitor to GND
B7	BK3OUT	Buck3 Regulator Output. Bypass with 10µF of capacitance to GND.
C1, C2	BAT	Battery Connection. Connect to positive battery terminal. Bypass with a minimum 1µF capacitance to GND.
C3	THM	Battery Temperature Measurement Thermistor Sensing Connection.
C4	TPU	Battery Temperature Measurement Pullup Resistor Connection.
C6	MPC0	Multipurpose Control I/O 0. LDO3 direct control option.
C7	MPC2	Multipurpose Control I/O 2
C8	MPC3	Multipurpose Control I/O 3
D3	TPUEXT	External Voltage Connection to be used as Supply of the Battery Temperature Measurement Resistive Divider.
D6	PFN2	Configurable Power Mode Control Pin (e.g. $\overline{KOUT}$)
D7	MPC1	Multipurpose Control I/O 1. Buck-Boost FAST control option.
D8	SCL	I^2C Serial Clock Input
E1, E2	CHGIN	+28V/-5.5V Protected Charger Input. Bypass with 1µF capacitor to GND.
E3	CAP	Internal Reference Supply. Bypass with 1µF capacitor to GND.
E6	$\overline{RST}$	Reset Open-Drain Output. Active-low.
E7	PFN1	Configurable Power Mode Control Pin (e.g., $\overline{KIN}$).
E8	SDA	I^2C Serial Data Input / Open-Drain Output
F2	BK2OUT	Buck2 Regulator Output. Bypass with 10µF of capacitance to GND.
F3	L1IN	LDO1 Input. Bypass with 1µF capacitor to GND.
F4	LSW1IN	Load Switch 1 Input
F5	LSW2IN	Load Switch 2 Input
F6	IVMON	Voltages and Charging Current Monitor Multiplexer Output

Pin Description (continued)

PIN	NAME	FUNCTION
F7	BK1OUT	Buck1 Regulator Output. Bypass with 10µF of capacitance to GND.
G1	BK2LX	Buck2 Regulator Switch. Connect through 2.2µH inductor to BK2OUT.
G3	L1OUT	LDO1 Output. Bypass with 1µF of capacitance to GND.
G4	LSW1OUT	Load Switch 1 Output
G5	LSW2OUT	Load Switch 2 Output
G6	$\overline{INT}$	Interrupt Open-Drain Output. Active-low.
G8	BK1LX	Buck1 Regulator Switch. Connect through 2.2µH inductor to BK1OUT.

Detailed Description

Power Regulation

The MAX20345 features three high-efficiency, low-quiescent-current buck regulators, a Buck-Boost regulator, two load switches, and three low-quiescent-current, low-dropout (LDO) linear regulators that are configurable as load switches. Excellent light-load efficiency allows the switching regulators to run continuously without significant energy cost. The buck and Buck-Boost regulators can operate in a fixed peak current mode for low-current applications, as well as an adaptive peak current mode to improve load regulation, and extend the high-efficiency range.

LDO3 MPC0 Control

All of MAX20345s LDOs can be enabled using an MPC input and are configurable as load switches. The low voltage LDO3 offers an additional, on-the-fly configuration option. Setting the LDO3_MPC0CNT bit to 1 configures LDO3 to be adjusted by MPC0 based on the state of LDO3_MPC0CNF. If LDO3_MPC0CNF = 0, MPC0 toggles LDO3 between LDO mode and switch mode. If LDO3_MPC0CNF = 1, then MPC0 enables or disables LDO3 in switch mode. Using this MPC control allows the state of LDO3 to be changed much more quickly than through I^2C writes, on the order of microseconds. Rapid control of LDO3 supports applications that require minimal delays. For example, quickly increasing the LDO3 voltage reduces the time required for an application processor to transition from a low-power sleep mode to a higher voltage active state.

Load Switches

The MAX20345s load switches allow a system to disconnect loads when inactive to reduce quiescent current. Each load switch initially behaves as a constant current source with the value I_{LSW_START}. A switch charges its output until it meets the condition $V_{LSW\_IN} - V_{LSW\_OUT} < V_{LSW\_PROT}$. Once the condition is met, the switch turns fully on and connects LSW_IN to LSW_OUT. If this condition is not met within the startup time-out t_{STUP_LSW}, the switch attempts to turn on after a retry delay t_{RTRY_LSW}.

Both switches feature optional voltage protection at their inputs. A protection comparator monitors the difference between the input and output voltages. If the difference exceeds V_{SW_PROT}, the switch is opened to protect downstream circuitry. The comparator can be disabled with the LSW_LowIq bit to reduce quiescent current.

Power Switch and Reset Control

The MAX20345 features a power switch that provides the ability to execute a reset sequence or to turn off the main system power and enter Off mode to extend battery life. Shutdown and reset events are triggered by an external control through the power function (PFN) control inputs, I^2C commands, or if other conditions are met. The behavior of the PFN pins is preconfigured to support one of the multiple types of wearable application cases. Table 1 describes the behavior of the PFN1 and PFN2 pins based on the PwrRstCfg[3:0] bits, while Figure 1a through Figure 1g shows basic flow diagrams associated with each mode.

A soft-reset sends a 10ms pulse on $\overline{RST}$ and either leaves register settings unchanged or resets them to their default values depending on the device version (see Table 3 for device settings). A hard reset on any device initiates a complete power-on reset (POR) sequence.

The device enters Off mode on cold boot (initial battery attach, V_{CHGIN} = 0V), in response to a power-off I^2C command or to a valid PFN signal based on the PwrRstCfg[3:0] setting, in the case of an undervoltage (UVLO) condition on SYS and in the case of an overcurrent (OCP) condition on BAT. When the device is in Off mode, the BAT-SYS connection is opened and all functions are disabled except for the power function controller and LDO1 (if configured as always-on).

The MAX20345 exits Off mode and turns the main power back on when there is a qualified PFN1 signal (PwrRstCfg[3:0] = 0000, 0001, 0110, 0111, 1000, 1001, 1010) or when a valid voltage is applied to CHGIN. In the powered-on state, the SYS node is enabled and other functions can be controlled through the I^2C registers. When the power-on event occurs, the power path to SYS is enabled after a 30ms delay. Figure 2 illustrates a complete boot sequence coming out of the Off state.

Table 1. PwrRstCfg Settings

PwrRstCfg[3:0]	MODE	PFN1 FUNCTION	PFN2 FUNCTION	BEHAVIOR
0000	On/$\overline{Off}$	Enable	Manual $\overline{RESET}$	On/Off Mode with 10ms Debounce. PFN1 is the active-high on/off control input. PFN2 is the active-low soft-reset input.
0001	$\overline{On}$/Off	Disable	Manual $\overline{RESET}$	On/Off Mode with 10ms Debounce. PFN1 is the active-low on/off control input. PFN2 is the active-low soft-reset input.
0010	Always-On	Hard-Reset on Rising Edge	Soft-Reset on Rising Edge	Always-On Mode. A rising edge on PFN1 generates a hard-reset after a 200ms delay. A rising edge on PFN2 generates a soft-reset after a 200ms delay. The device can only enter the off state by writing to the PwrCmd register.
0011	Always-On	Hard-Reset on Falling Edge	Soft-Reset on Falling Edge	Always-On Mode. A falling edge on PFN1 generates a hard-reset after a 200ms delay. A falling edge on PFN2 generates a soft-reset after a 200ms delay. The device can only enter the off state by writing to the PwrCmd register.
0100	Always-On	Hard-Reset when High on CHGIN Insertion	Soft-Reset when High on CHGIN Insertion	Always-On Mode. Holding PFN1 high during a CHGIN insertion generates a hard-reset after a 200ms delay. Holding PFN2 high during a CHGIN insertion triggers a soft-reset after a 200ms delay. The device can only enter the off state by writing to the PwrCmd register.
0101	Always-On	Hard-Reset when Low on CHGIN Insertion	Soft-Reset when Low on CHGIN Insertion	Always-On Mode. Holding PFN1 low during a CHGIN insertion generates a hard-reset after a 200ms delay. Holding PFN2 low during a CHGIN insertion triggers a soft-reset after a 200ms delay. The device can only enter the off state by writing to the PwrCmd register.
0110	$\overline{KIN}$	$\overline{KIN}$	KOUT	On/Off Through Key Presses. PFN1 is the active-low $\overline{KIN}$ button. PFN2 is the open-drain KOUT output, which buffers the $\overline{KIN}$ input. The device enters on mode through a short (400ms) KIN press or when a valid CHGIN voltage is present. The device enters off mode through a long (> 12s) $\overline{KIN}$ press or through the PwrCmd register.
0111	$\overline{KIN}$	$\overline{KIN}$	KOUT	On/Reset Through Key Presses. PFN1 is the active-low $\overline{KIN}$ button. PFN2 is the open-drain KOUT output, which buffers the $\overline{KIN}$ input. The device enters on mode through a long (> 3s) $\overline{KIN}$ press or when a valid CHGIN voltage is present. A long (> 12s) $\overline{KIN}$ press generates a soft-reset. The device can only enter the off state by writing to the PwrCmd register.

Table 1. PwrRstCfg Settings (continued)

PwrRstCfg[3:0]	MODE	PFN1 FUNCTION	PFN2 FUNCTION	BEHAVIOR
1000	$\overline{KIN}$	$\overline{KIN}$	Manual $\overline{RESET}$	On/Reset Through Key Presses. PFN1 is the active-low $\overline{KIN}$ button. The device enters on mode through a long (3s) $\overline{KIN}$ press or when a valid CHGIN voltage is present. A long (> 12s) PFN2 press generates a soft-reset. The device can only enter the off state by writing to the PwrCmd register.
1001	Always-On	Hard-Reset when High on CHGIN Insertion or Abort Hard-Reset when Low	Soft-Reset when High on CHGIN Insertion or Abort Soft-Reset when Low	Always-On Mode. The device can only enter the on state when a valid CHGIN voltage is present. Holding PFN1 high during a CHGIN insertion generates a hard-reset after a 15 second delay. If PFN1 is brought low during this delay (10ms debounce), the hard-reset is aborted. Holding PFN2 high during a CHGIN insertion generates a soft-reset after a 15 second delay. If PFN2 is brought low during this delay (10ms debounce), the hard-reset is aborted.
1010	Always-On	Hard-Reset when Low on CHGIN Insertion or Abort Hard-Reset when High	Soft-Reset when Low on CHGIN Insertion or Abort Soft-Reset when High	Always-On Mode. The device can only enter the on state when a valid CHGIN voltage is present. Holding PFN1 low during a CHGIN insertion generates a hard-reset after a 15 second delay. If PFN1 is brought high during this delay (10ms debounce), the hard-reset is aborted. Holding PFN2 low during a CHGIN insertion generates a soft-reset after a 15 second delay. If PFN2 is brought high during this delay (10ms debounce), the hard-reset is aborted.
1011-1111	RFU			

PwrRstCfg Diagrams

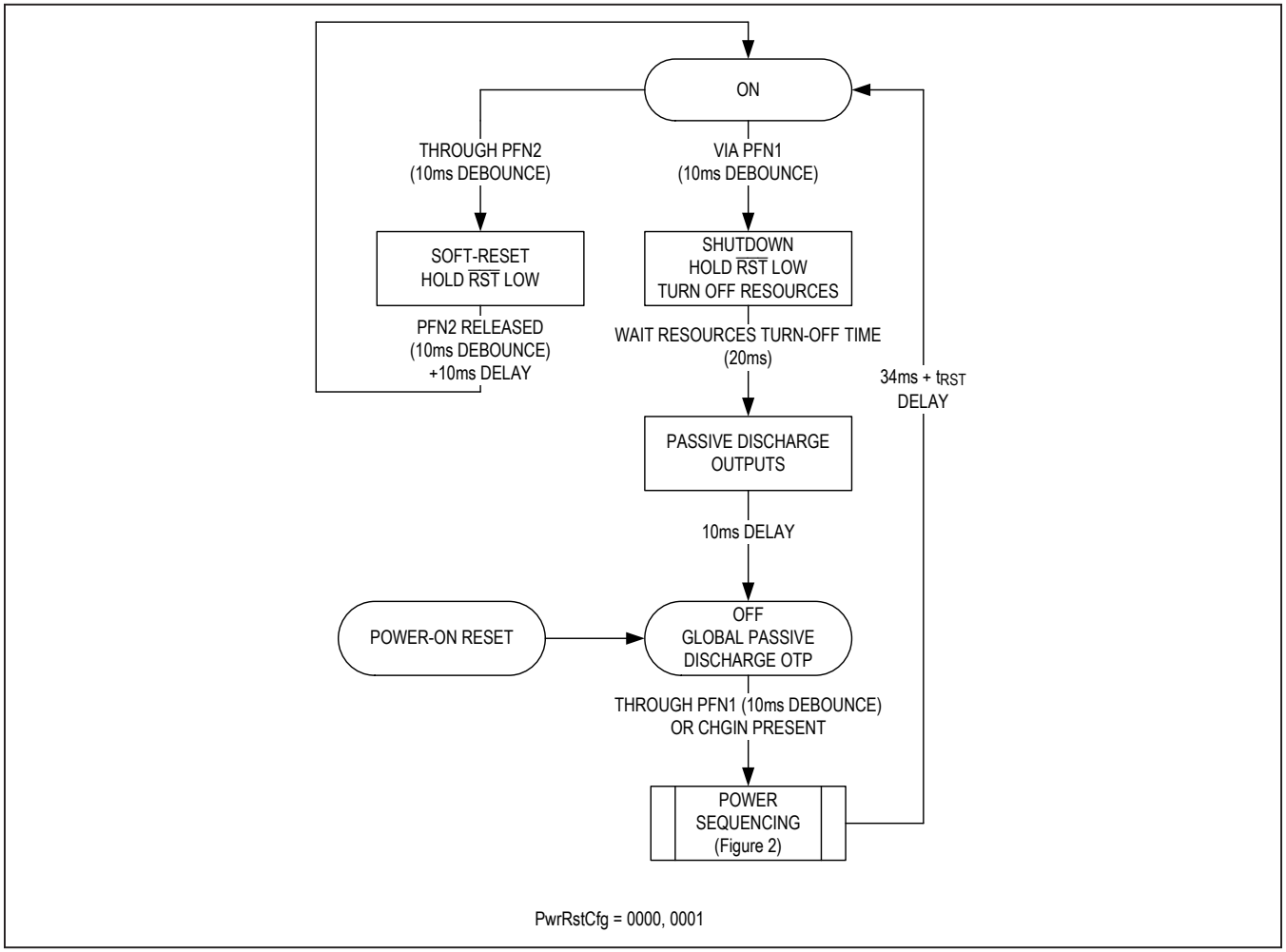


Figure 1a. PrwRstCfg = 0000,0001

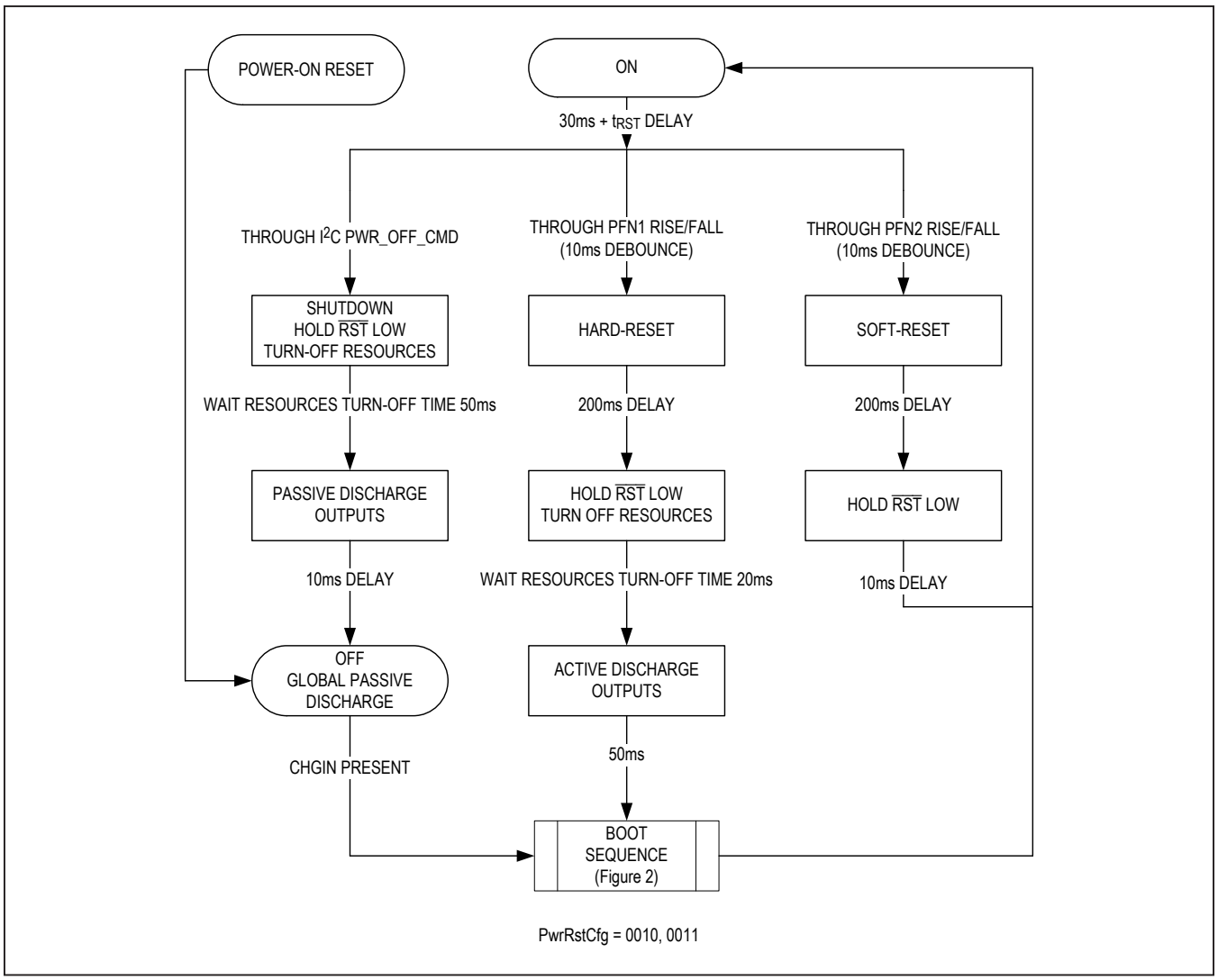


Figure 1b. PrwRstCfg = 0010, 0011

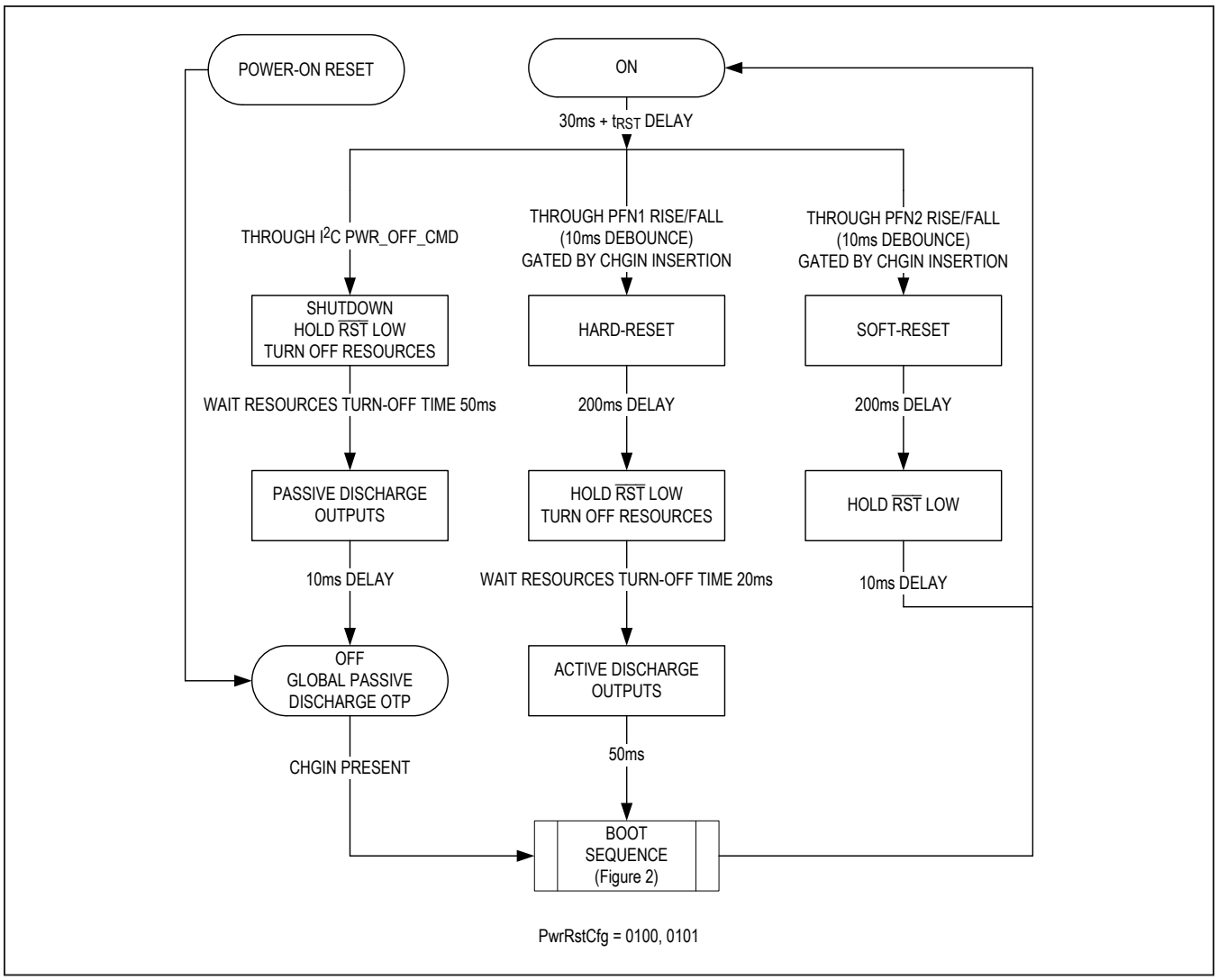


Figure 1c. PwrRstCfg = 0100, 0101

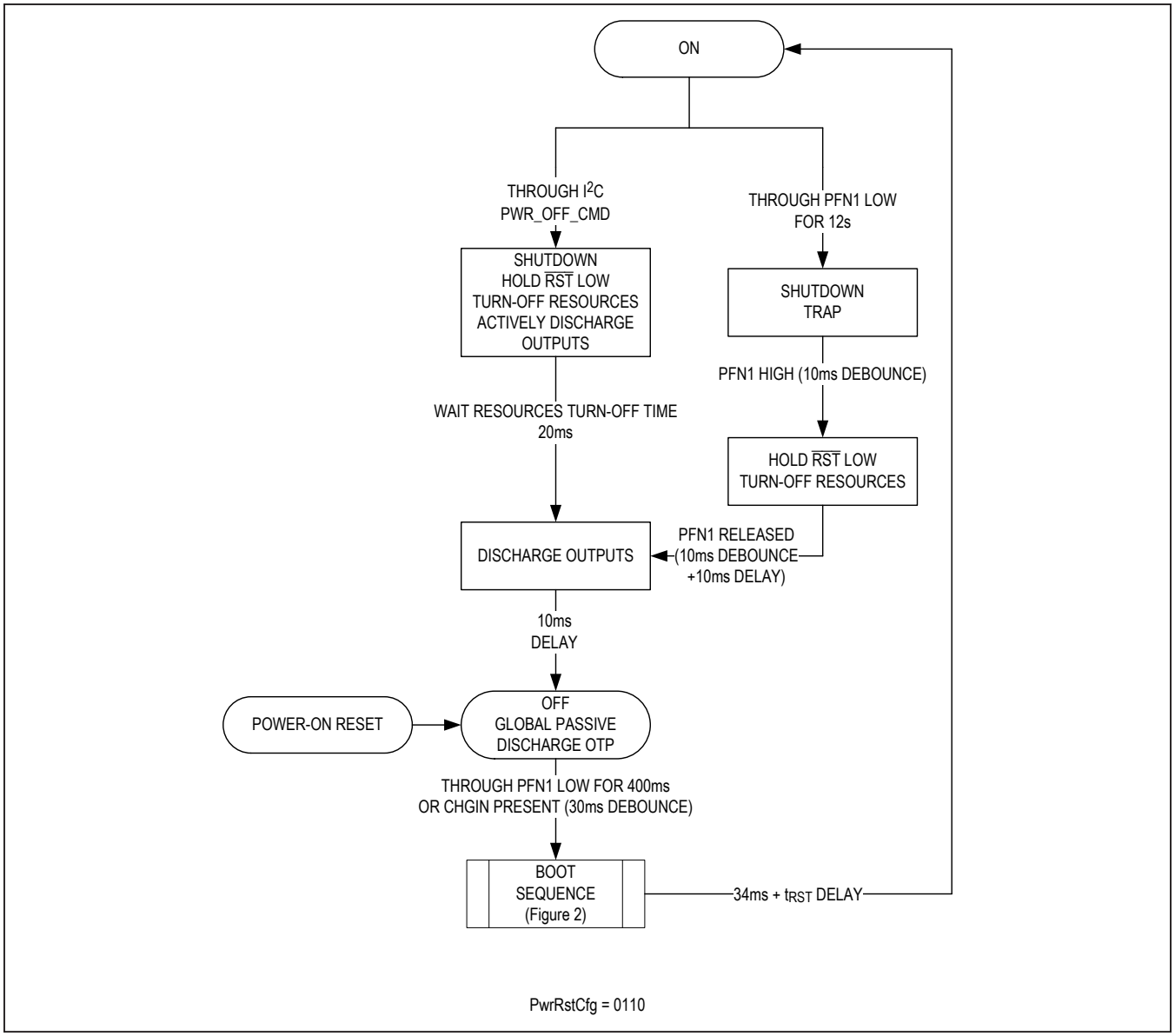


Figure 1d. PwrRstCfg = 0110

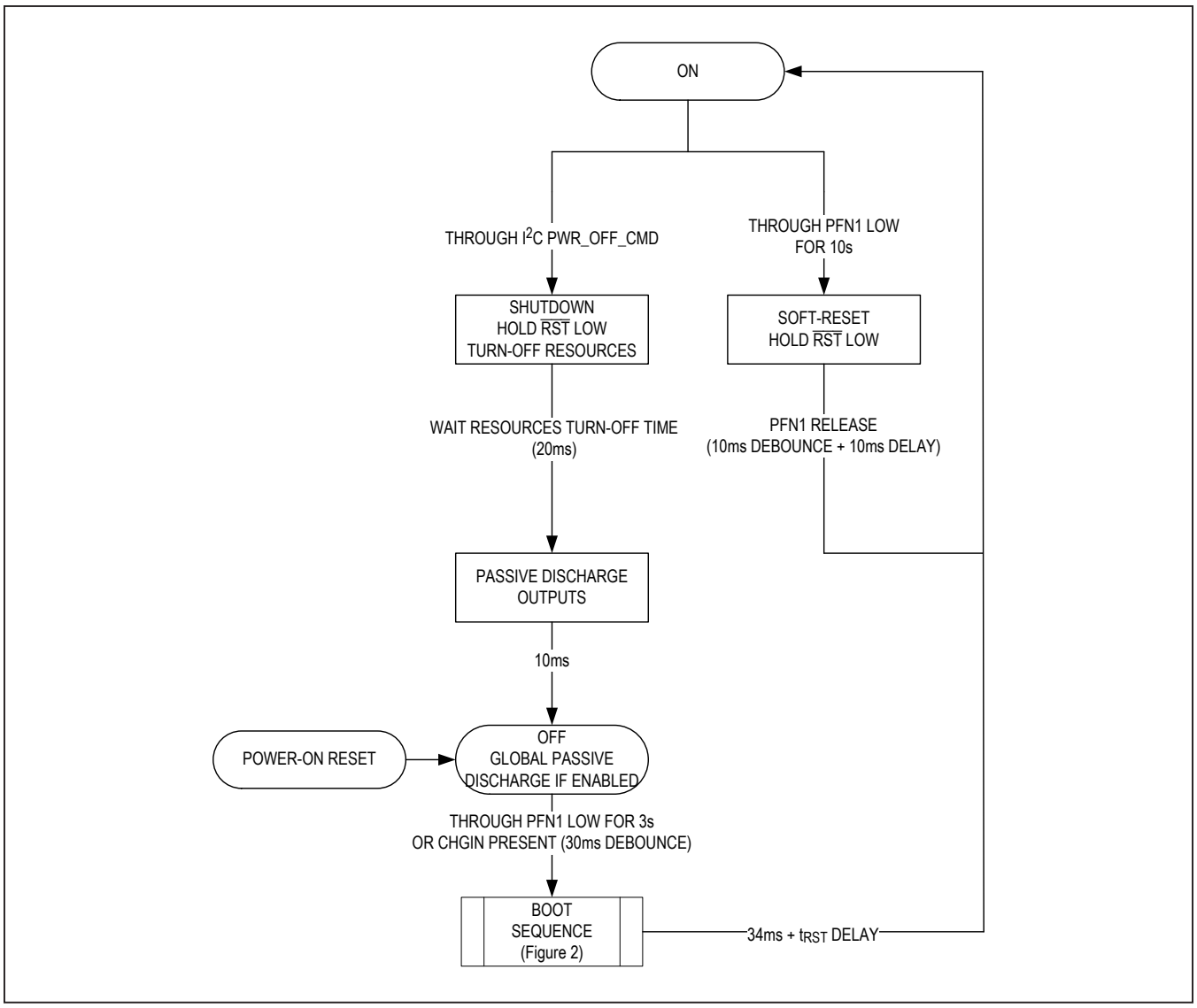


Figure 1e. PwrRstCfg = 0111

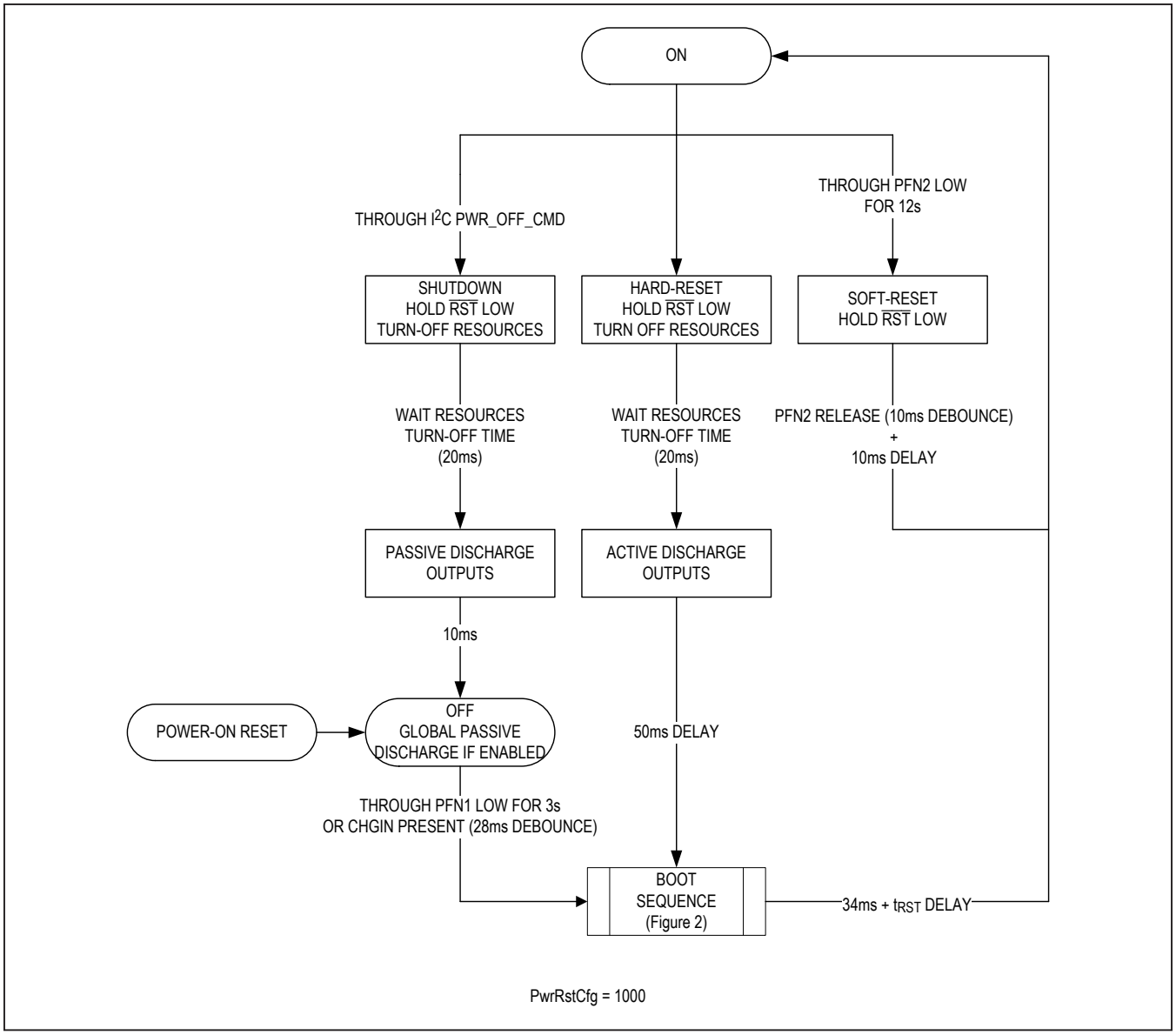


Figure 1f. PwrRstCfg = 1000

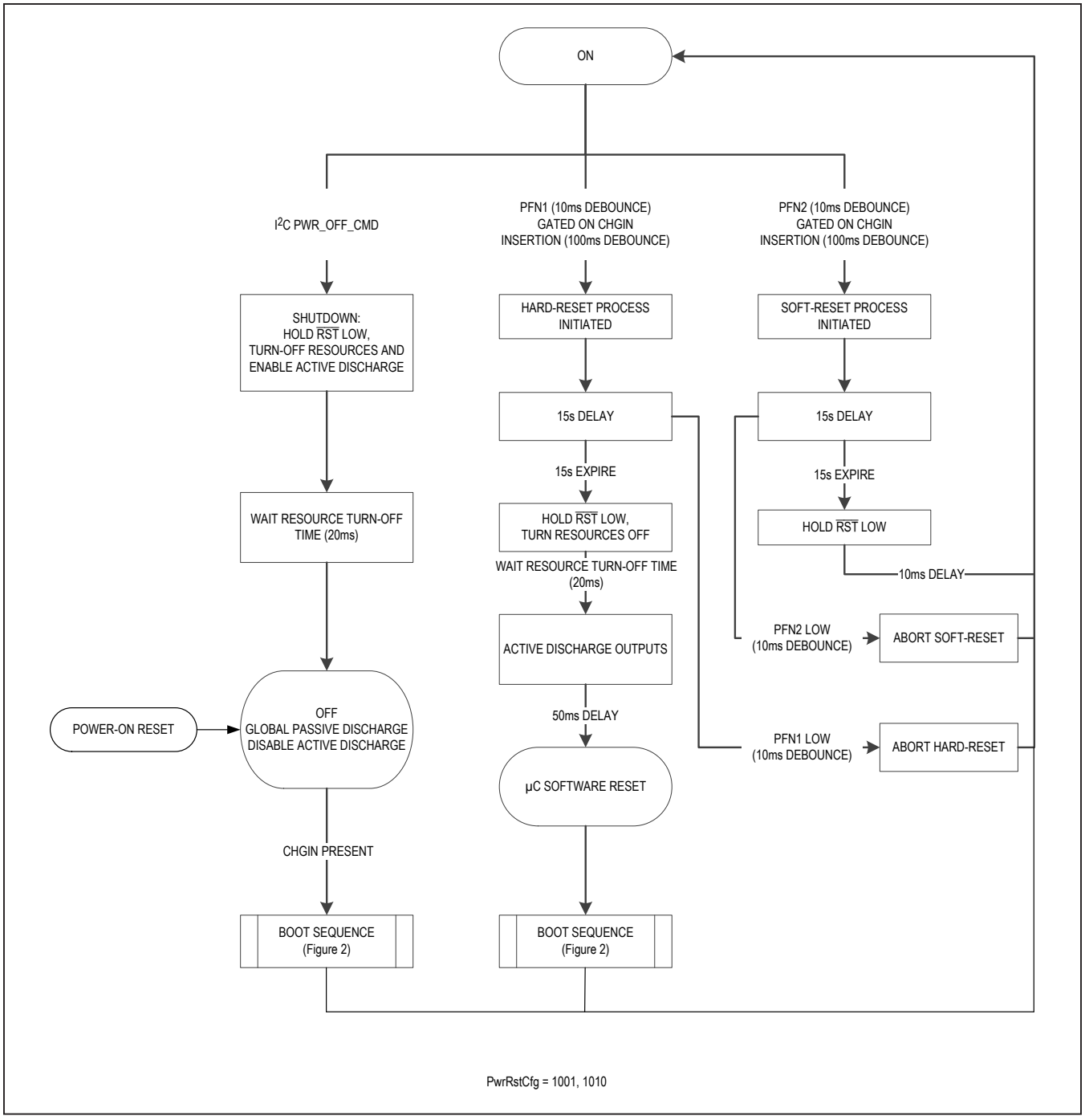


Figure 1g. PwrRstCfg = 1001, 1010

Boot Sequence

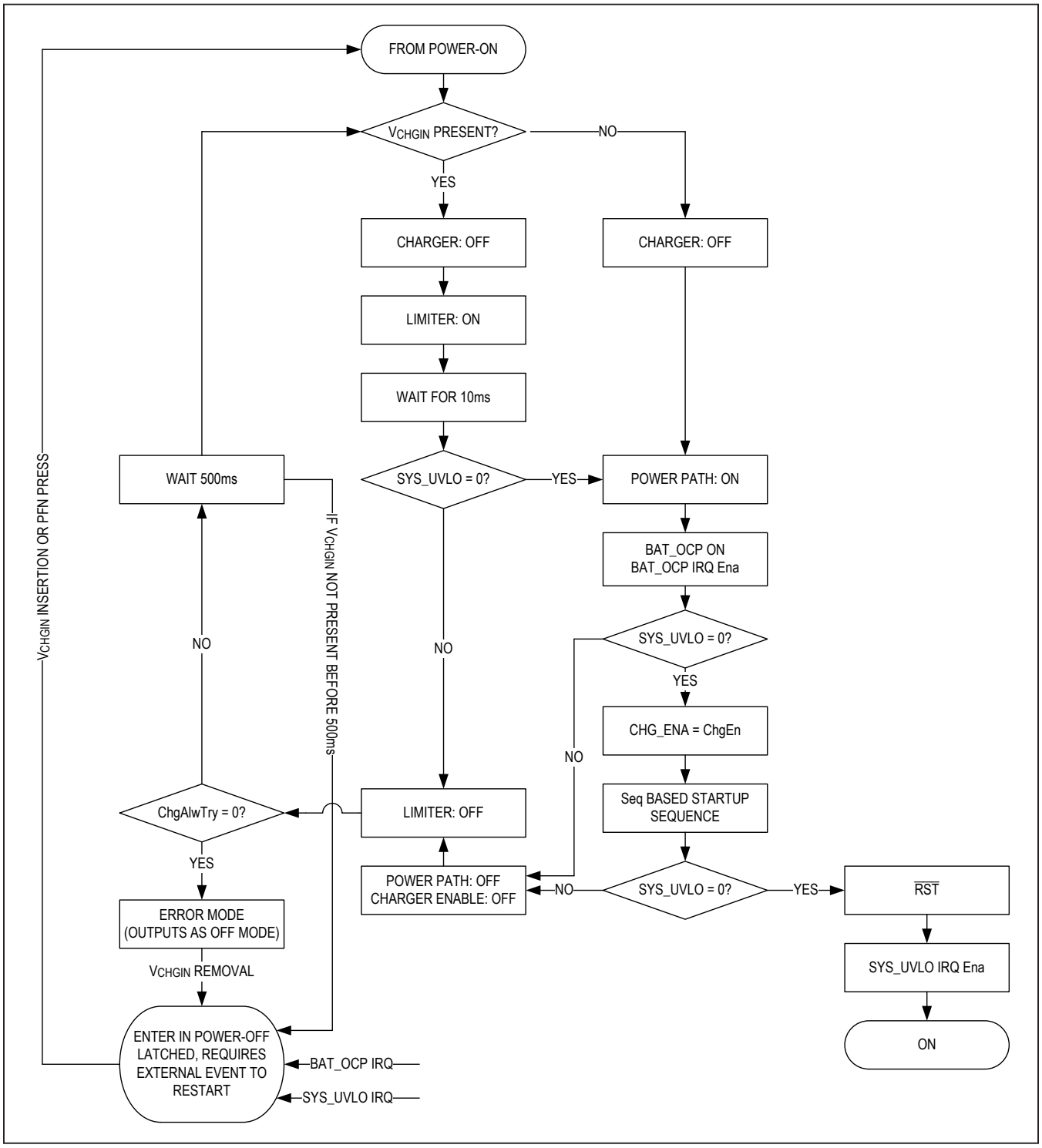


Figure 2. The MAX20345 Boot Sequence

Power Sequencing

The sequencing of the switching regulators, LDOs, and load switches during power-on is configurable. See each function's sequencing bits for details. Regulators and switches can turn on at one of three points during the power-on process: 45ms after the power-on event, at the time the $\overline{RST}$ signal is released, or at two points in between. The two points between the 45ms delay and the $\overline{RST}$ rising edge are fixed proportionally to the duration of the power-on reset (POR) process boot delay (t_{RST}). The value of the t_{RST} delay ranges from 80ms to 420ms and is stored in the BootDly[1:0] bits of register 0x4D. The timing relationship is presented graphically in Figure 3.

Alternatively, the regulators and switches can remain off by default to be turned on manually with an I^2C command after $\overline{RST}$ is released. LDO1 can be configured to be always-on as long as SYS or BAT is present.

The SYS voltage is monitored during the power-on sequence. If V_{SYS} falls below V_{SYS_UVLO} during the sequencing process with a valid voltage at CHGIN, the process repeats from the point where SYS was enabled to allow more time for the voltage to stabilize. If there is not a valid voltage at CHGIN, the device returns to the OFF state to avoid draining the battery. Power is also turned off if a current greater than IBatOc is sunk from BAT for more than $t_{BAT\_OC\_D}$.

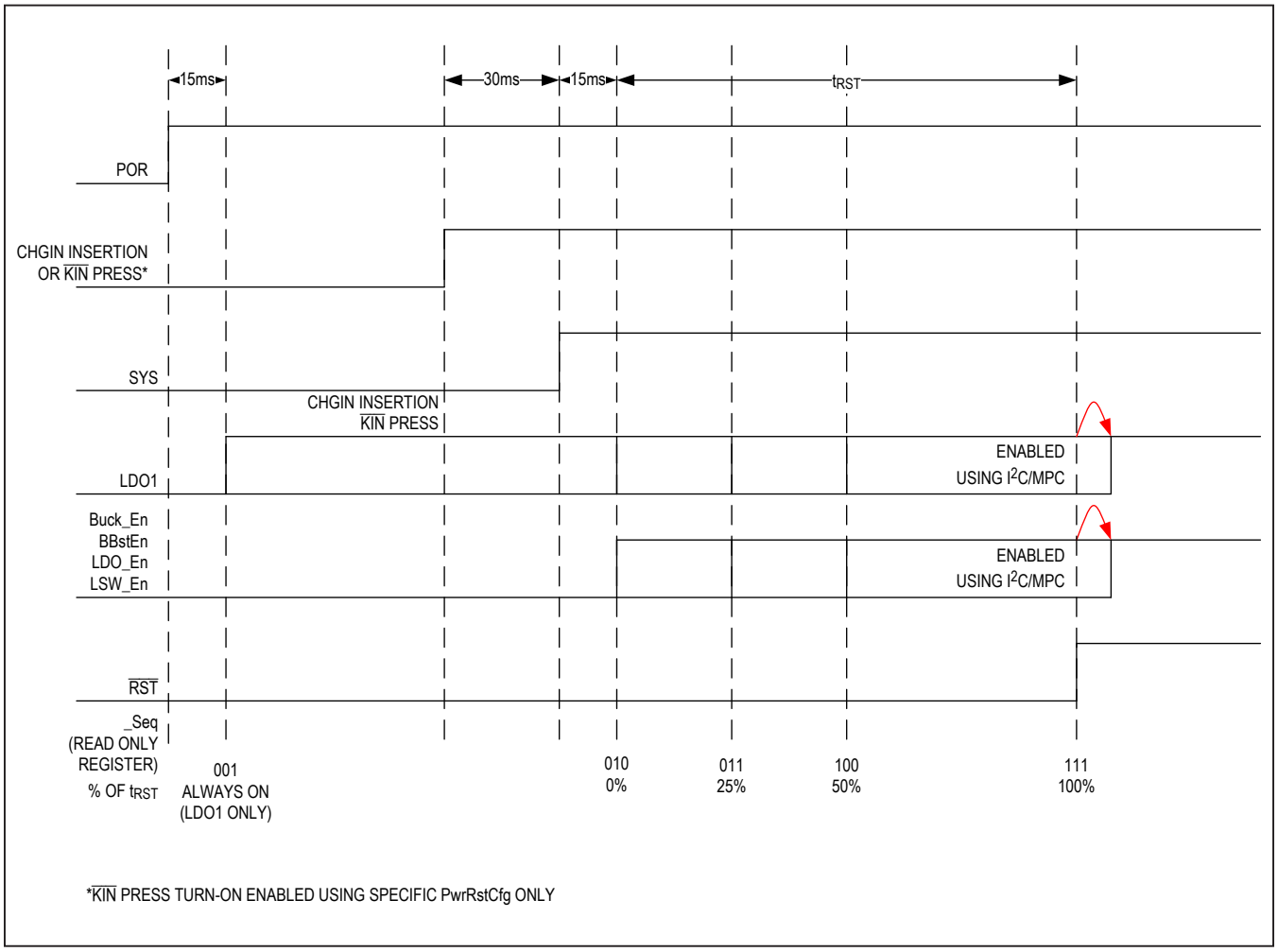


Figure 3. Reset Sequence Programming

System Load Switch

An internal 80mΩ (typ) MOSFET connects BAT to SYS when no voltage source is available on CHGIN. When an external source is detected at CHGIN, this switch opens and SYS is powered from the input source through the input current limiter. The SYS-to-BAT switch also prevents V_{SYS} from falling below V_{BAT} when the system load exceeds the input current limit. If V_{SYS} drops to V_{BAT} due to the current limit, the BAT-SYS switch turns on so the load is supported by the battery. If the system load continuously exceeds the input current limit, the battery is not charged. This is useful for handling loads that are nominally below the input current limit but have high current peaks exceeding the input current limit. During these peaks, battery energy is used, but at all other times the battery charges.

Smart Power Selector

The smart power selector seamlessly distributes power from the external CHGIN input to the BAT and SYS nodes. With both an external adapter and battery connected, the smart power selector basic functions are:

- When the system load requirements are less than the input current limit, the battery is charged with residual power from the input.
- When the system load requirements exceed the input current limit, the battery supplies supplemental current to the load.
- When the battery is connected and there is no external power input, the system is powered from the battery.

Input Limiter

The input limiter distributes power from the external adapter to the system load and battery charger. In addition to the input limiter's primary function of passing power to the system load and charger, it performs several additional functions to optimize use of available power.

Invalid CHGIN Voltage Protection

If CHGIN is above the overvoltage threshold V_{CHGIN_OV}, the device enters overvoltage lockout (OVLO). OVLO protects the MAX20345 and downstream circuitry from high-voltage stress up to +28V. During OVLO, the internal circuit remains powered and an interrupt is sent to the host. The negative voltage protection down to -5.5V disconnects CHGIN and the device is powered only by BAT. The charger turns off and the system load switch closes, allowing the battery to power SYS. CHGIN is also invalid if it is less than V_{BAT}, or less than the V_{CHGIN_DET} threshold. With an invalid input voltage, the BAT-SYS load switch closes and allows the battery to power SYS.

CHGIN Input Current Limit

The CHGIN input current is limited to prevent input overload. The input current limit I_{LIM} is I^2C controlled through paramter ILimCntl[2:0]. To accommodate systems with a high in-rush current, the limiter includes a blanking time t_{ILIM_BLANK}, I^2C programmable through the parameter ILimBlank[1:0], during which the input current limit increases to I_{LIM_MAX}.

Thermal Limiting

In case the die temperature (T_{DIE}) exceeds the T_{CHG_LIM}, the MAX20345 attempts to limit temperature increase by reducing the input current from CHGIN. In particular, the system load has priority over the charger current, so the input current is first reduced by lowering the charge current. If the junction temperature continues to rise and reaches the maximum operating limit T_{CHG_SHDN}, no input current is drawn from CHGIN and the battery powers the entire system load.

Adaptive Battery Charging

While the system is powered from CHGIN, the charger draws power from SYS to charge the battery. If the total load exceeds the input current limit, an adaptive charger control loop reduces charge current to prevent V_{SYS} from collapsing below the maximum between V_{SYS_LIM}, I^2C programmable through the SysMin[2:0] parameter, and $V_{SYS\_BAT\_LIM}$ values. When the charge current is reduced below 50% (I_{FCHG_TEXT} threshold) due to V_{SYS_LIM}/$V_{SYS\_BAT\_LIM}$ or T_{CHG_LIM} limits, the timer clock operates at half speed. When the charge current is reduced below 20% (I_{FCHG_TSUS} threshold) due to V_{SYS_LIM}/$V_{SYS\_BAT\_LIM}$ or T_{CHG_LIM} limits, the timer clock is paused.

Fast Charge Current Setting

The MAX20345 uses an external resistor connected from ISET to GND to set the fast-charge current I_{FCHG}. The precharge, I_{PCHG}, and charge-done (I_{CHG_DONE}) currents are I^2C programmed using IPChg[1:0] and IChgDone[1:0] parameters, respectively, as a percentage of this value. The fast-charge current resistor can be calculated as:

$$R_{ISET} = K_{ISET} \times V_{ISET}/I_{FCHG}$$

where K_{ISET} has a typical value of 2000A/A and V_{ISET} has a typical value of +1V. The range of acceptable resistors for R_{ISET} is 4kΩ to 400kΩ. A capacitive load on ISET can cause instability of the charger if the condition (C_{ISET} < 5µs/R_{ISET}) pF is violated.

JEITA Monitoring with Charger Control

To enhance safety when charging Li+ batteries, the MAX20345 includes a JEITA compliant temperature monitoring. A resistive divider is formed on THM by attaching a pullup resistor to TPU and connecting the thermistor of a battery-pack (do not exceed 2mA load on TPU). TPU is internally connected to the internal reference CAP. The divider output is read by internal comparators when JEITA monitoring is enabled and the resulting temperature measurement places the battery into one of five temperature zones: cold, cool, room, warm, and hot. Charging is always inhibited in cold and hot regions or if the thermistor is not detected, while charging behavior is configurable in warm, room, and cool regions using the I^2C-controlled ThmEn[2:0] parameter. In particular, the battery regulation voltage can be reduced to $V_{BAT\_REG\_JTA}$ value using the I^2C-programmed Cool/Room/WarmBatReg[1:0] parameters, while the fast-charge current can be reduced to I_{FCHG_JTA} value using the I^2C-programmed Cool/Room/WarmIFChg[2:0] parameters. Charging can also be inhibited in cool and warm regions using ThmEn[2:0].

THM One-Shot Measurement

Although the MON MUX can route the THM voltage to IVMON with any divider setting, only the 1:1 divider should be used. This ensures the MUX divider impedance does not interfere with the output of the thermistor resistive divider. By default, the thermistor pullup TPU is internally connected to CAP. This does not pose any problem if the application ADC can tolerate the CAP voltage level. If the application ADC requires a lower voltage, however, THM must be sampled using a one-shot measurement procedure.

If a lower voltage reference is needed for thermistor monitoring, an external reference should be connected to TPUEXT and the one-shot THM measurement command should be used to measure the thermistor voltage. When the one-shot is triggered, the MAX20345 performs the following sequence of actions:

- The internal JEITA settings are stored to continue charging in the last sampled temperature region
- The MON MUX is forced into its Hi-Z state
- The internal TPU connection is switched from CAP to TPUEXT
- IVMON is set to output THM at a 1:1 ratio
- IVMON passes THM through for 500ms
- The MON MUX is forced into its Hi-Z state
- The internal TPU connection is switched back from TPUEXT to CAP
- The MON MUX returns to its last state before the one-shot

The command is triggered by a rising edge of ThmtoMonEna. The application ADC has 500ms (typ) to take a THM reading before the one-shot expires and the MON MUX returns to its previous state. A rising edge on ThmtoMonAbr aborts the one-shot procedure and returns the TPU reference to CAP.

Step Charging

Lithium batteries suffer capacity degradation over their lifetimes. One of the primary causes of degradation over the lifetime of a battery is due to an effect called lithium plating which describes the formation of metallic lithium on the anode of the battery. Lithium plating has many causes, but one of the most common is when the battery is charged at high rates relative to the capacity of the battery when the battery is at a high state of charge (SOC). To combat this effect, the MAX20345 includes a step charge function. This function allows the user to select a voltage threshold at which the charge current can be reduced in order to avoid lithium plating and prolong the lifetime of the battery. The settings of this function can be found in the StepChgCfg0 and StepChgCfg1 registers. The ChgStepRise[3:0] field allows the setting of the rising voltage V_{BAT_STPCHG} at which the charge current should be reduced. The ChgIStep[2:0] field sets the percentage I_{FCHG_STPCHG} of the full fast-charge current to which the charger should be set when the battery is above the V_{BAT_STPCHG} value specified with ChgStepRise[3:0]. Lastly, the ChgStepHyst[2:0] field sets the $V_{BAT\_STPCHG\_H}$ hysteresis for the step charge function in order to avoid oscillations in case a high battery impedance causes the voltage to fall a large amount upon reduction of the battery current. If this function is not desirable, set the ChgIStep[2:0] field to 100% ("111") to disable it.

In case both JEITA and Step-Charging related fast-charge current reductions are active, the minimum between the two is selected and applied.

Battery Charger State Diagram

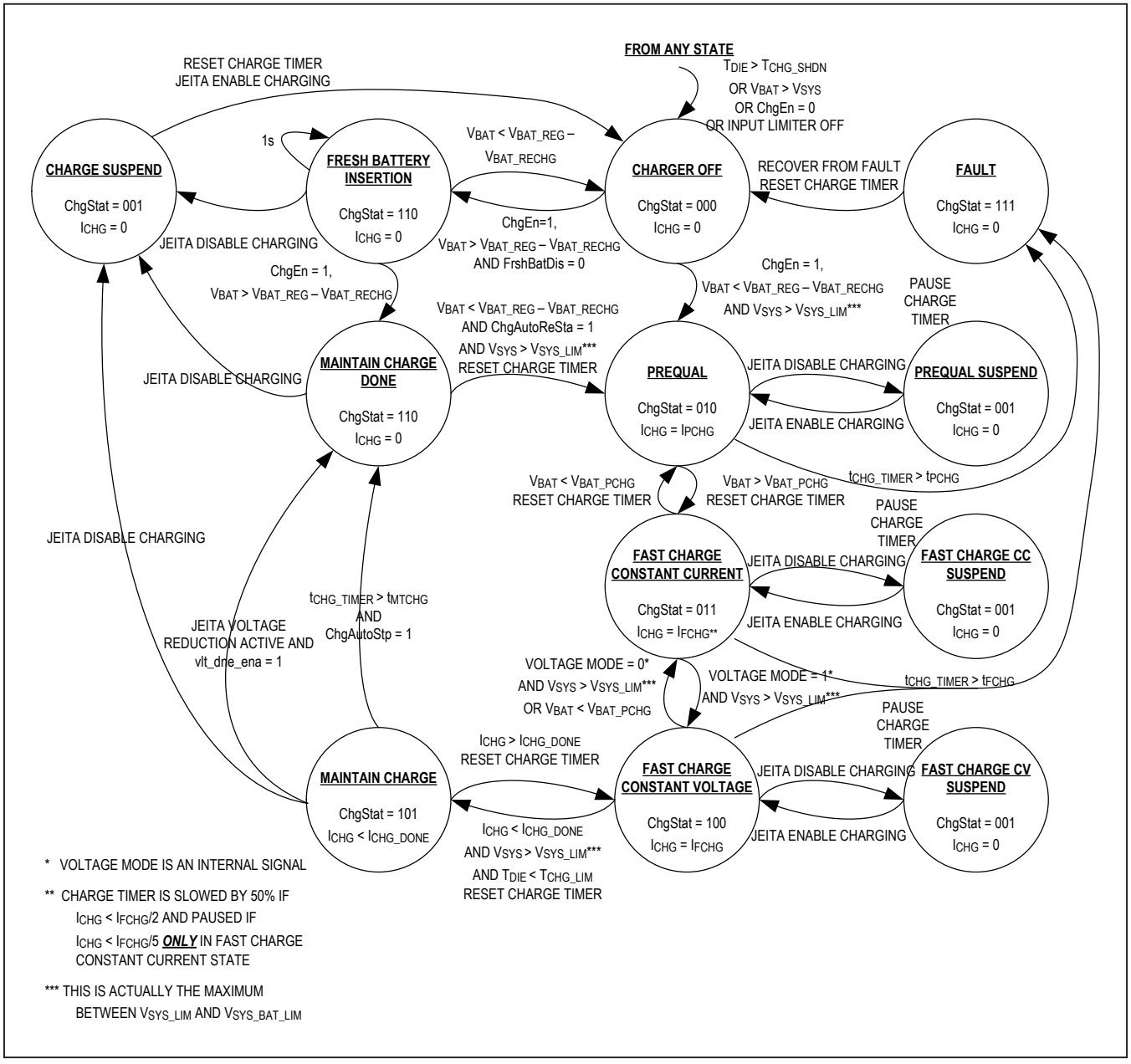


Figure 4. Battery Charger State Diagram

Function Locking

All regulator voltages and the end-of-charge behavior of the charger can be locked. I2C writes to a locked bitfield have no effect. To lock a function, its lock mask must be removed in the LockMsk register. To remove the lock mask, set the corresponding function's mask bit to 0. By writing the lock password 0xAA to the LockUnlock register, all unmasked functions are locked. To unlock functions, repeat the mask/unmask process and write the unlock password 0x55 to the LockUnlock register.

Monitor MUX

In order to simplify system monitoring, the MAX20345 includes a voltage monitor multiplexer (MUX). The MUX, I2C controlled using the MONCntl[3:0] parameter, connects the IVMON pin to the scaled value of one of the seven voltage regulators, THM, TPU, BAT, or SYS. A resistive divider scales the selected voltage to one of four ratios determined by MONRatioCfg[1:0]. Because the MUX can only tolerate voltages up to +5.5V, V_{CHGIN} is not available to MON.

Additionally, the ISET voltage is available to monitor the charging current according to the following equation:

$V_{ISET} = I_{CHG} / (I_{CHG\_PROG} \times I_{CHG\_RED})$ [V]

where:

I_{CHG} = Actual charging current flowing into BAT

I_{CHG_PROG} = Either the fast charge or precharge programmed current

I_{CHG_RED} = Eventual reduction factor can be due to JEITA and/or Step-Charging (see ChgIStep[2:0] and Cool/Room/WarmIFChg[2:0] parameters). If neither JEITA nor Step-Charging current reduction is active, I_{CHG_RED} is equal to 1.

Buck-Boost Regulator

The MAX20345's Buck-Boost regulator provides a low-ripple voltage rail with the ability to boost the battery voltage to 5V. A higher voltage rail eliminates the need for an external regulator to supply systems that cannot otherwise operate from the battery's voltage level. This includes OHR systems with short wavelength LEDs that require large forward voltage drops.

Several controls optimize the efficiency and output noise of the regulator. These include peak current control and automatic peak and valley current adjustment. Additionally, the Buck-Boost regulator can operate in buck-only mode to increase efficiency when V_{BBOUT} is much lower than V_{SYS}.

The MAX20345 buck-boost is designed to be compatible with small case-size ceramic capacitors. As such, the device has low output capacitance requirements to accommodate the steep voltage derating of 0603 and 0402 (imperial) capacitors. The sample derating curve in Figure 5 presents the minimum capacitance required at OUT for a given maximum set output voltage.

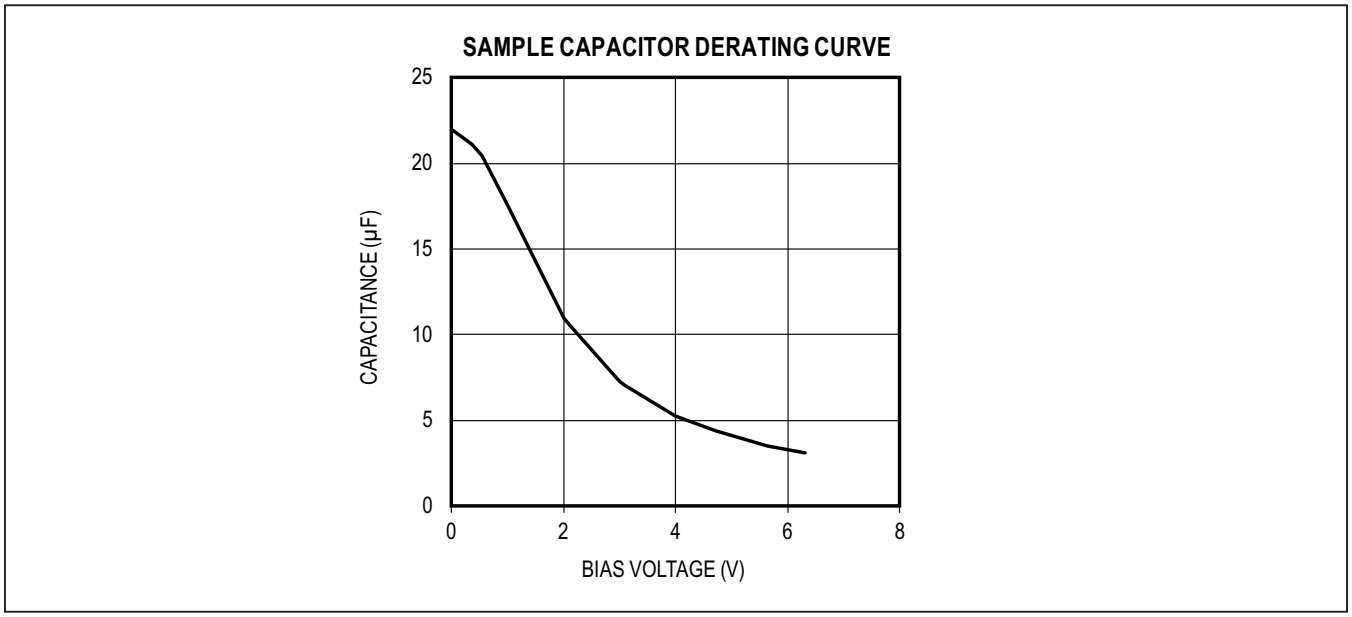


Figure 5. Capacitor Derating for Input and Output Capacitance on Buck-Boost

Architecture and Switching Phases

The Buck-Boost comprises a typical noninverting Buck-Boost topology. Figure 6 illustrates the regulator's basic structure with arrows depicting the current flow in each switching phase. Depending on the Buck-Boost configurations, the topology enters different sequences of phases to generate the desired output voltage. Only two switches are on in each phase.

- Phase 1: MP1 on, MP2 on. Inductor charges.
- Phase 2: MP1 on, MN2 on. Inductor charges.
- Phase 3: MN1 on, MP2 on. Inductor discharges.
- Phase 4: MN1 on, MN2 on. Freewheeling.

The Buck-Boost features a frequency comparator to monitor its switching frequency. Switching frequency increases as the load current increases. Under low loads, the Buck-Boost optimizes its feedback loop for low quiescent current. When load requirements increase the switching frequency to the f_{HIGH} threshold, the low-quiescent current mode is disabled to improve response time. The f_{HIGH} threshold is set by the BBFHighSH[1:0] in the BBstCfg1 register. Hysteresis prevents the Buck-Boost regulator from resuming the low-quiescent current mode until the switch frequency decreases to f_{HIGH} / 4.

Buck-Boost Mode

When BBstMode (register 0x31[1]) is 0, the regulator operates in Buck-Boost mode. The inductor charges in phase 2 up to BBstIPSet1 (register 0x33[3:0]). The Buck-Boost then transitions to phase 1. If $V_{SYS} > V_{BBOUT}$, the inductor continues charging until either the current reaches BBstIPSet1 + BBstIPSet2 (register 0x33[7:4]) or after a 500ns delay. If $V_{SYS} \le V_{BBOUT}$, the Buck-Boost waits for the 500ns delay to elapse or until the current drops to the valley limit. Next, the regulator enters phase 3 to discharge the inductor current to the valley limit. When the inductor current reaches the valley-current crossing threshold or falls below 0, the regulator freewheels in phase 4 until the next charge phase. When operating in continuous conduction mode (CCM), the Buck-Boost enters phase 4 for approximately 30ns if BBZCCmpEnb = 1. The Buck-Boost skips phase 4 when operating in CCM and BBZCCmpEnb = 0. The valley behavior is determined by BBZCCmpEnb (register 0x34[5]). Figure 7 shows the inductor current in Buck-Boost mode.

Buck-Only Mode

To maximize efficiency when $V_{SYS} > V_{BBOUT}$, the Buck-Boost regulator has a buck-only mode. When BBstMode = 1, the regulator behaves as a synchronous buck regulator. The inductor charges in phase 1 until the inductor current reaches BBstIPSet1. The regulator then transitions to phase 3 to provide a path to deliver the inductor current to the output. Figure 8 shows the inductor current in buck-only mode.

Buck-only mode reduces switching losses present in Buck-Boost mode. Buck-only mode should be used when V_{BBOUT} is always less than V_{SYS} to maximize efficiency.

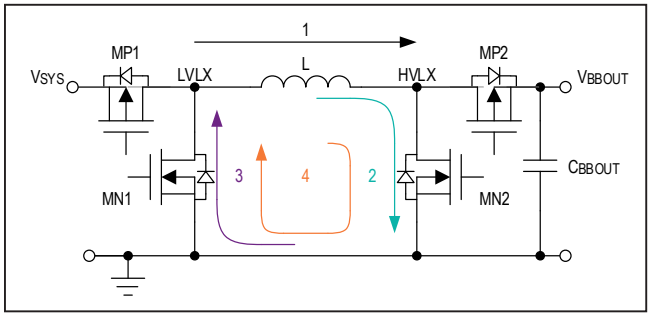


Figure 6. The Buck-Boost Regulator and Switching Phases

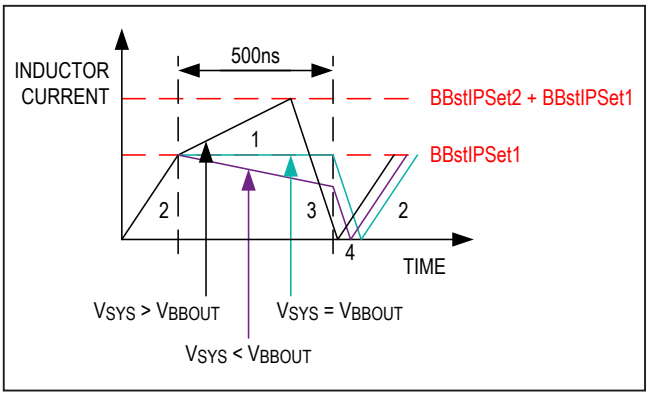


Figure 7. Buck-Boost Inductor Current in Buck-Boost Mode

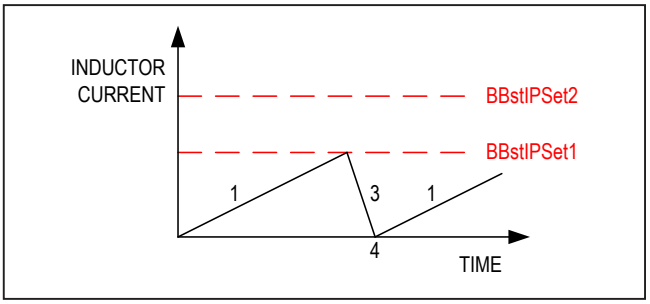


Figure 8. Buck-Boost Inductor Current in Buck-Only Mode

Inductor Peak and Valley Current Limits

The Buck-Boost regulator monitors the maximum and minimum values of the inductor current to control output noise and reduce switching losses. Peak and valley currents can be fixed to the values in BBstISet and 0mA, respectively, or allowed to change based on load requirements if BBstIPAdptDis (register 0x34[7]) = 0.

Peak currents are set in the BBstISet register. BBstIPSet1 controls the peak current when V_{SYS} < V_{BBOUT} and when the regulator is in buck-only mode. BBstIPSet2 sets a secondary current limit when V_{SYS} > V_{BBOUT} in Buck-Boost mode. The total inductor current limit when V_{SYS} > V_{BBOUT} is BBstIPSet1 + BBstIPSet2. The Buck-Boost regulator transitions to phase 3 if the inductor current reaches BBstIPSet2 before the 500ns timeout has elapsed. Minimizing the difference between BBstIPSet1 and BBstIPSet2 reduces the output ripple, but decreases efficiency. Care must be taken to optimize the peak current settings to keep a low output ripple while maximizing efficiency. Figure 9 presents the safe operating area of BBstIPSet2 with respect to BBstIPSet1. Selecting values lower than those of Figure 9 for a given BBstIPSet1 value may reduce efficiency and increase output ripple.

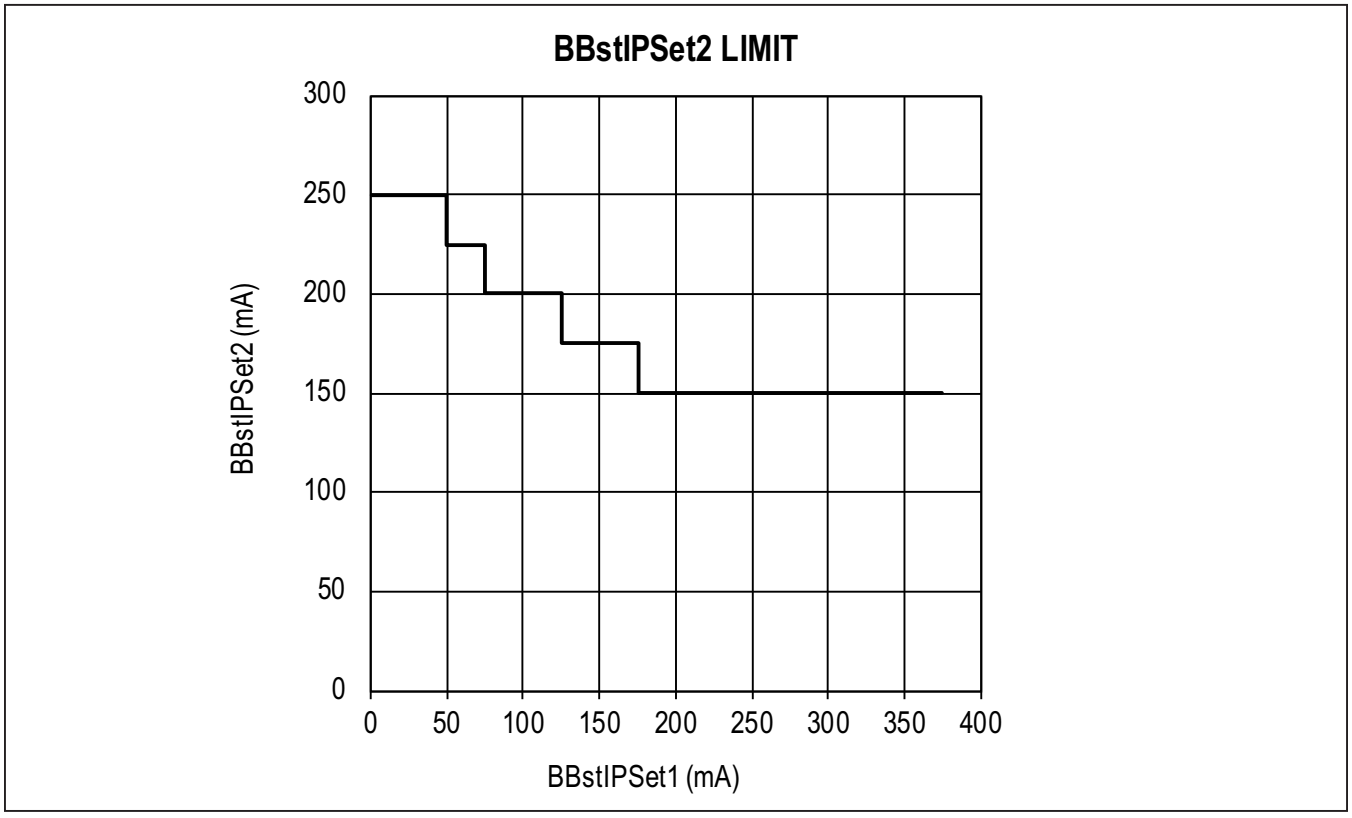


Figure 9. Minimum BBstIPSet2 Limit for a Given BBstIPSet1 Setting

Figure 10 is a graphical guide to selecting combinations of BBstPSet1 and BBstIPSet2 to maximize efficiency for specific BBstVSet values.

When BBstIPAdptDis = 0, the regulator automatically increases the peak current limits when the load increases to improve load regulation and efficiency at high loads. When BBZCCmpEnb = 1, the Buck-Boost operates with peak and valley current limits. In discontinuous conduction mode (DCM), the valley limit is 0mA and acts as a zero crossing. In CCM mode, the peak and valley limits are automatically adjusted by the voltage loop if BBstIPAdptDis = 0.

When BBZCCmpEnb = 0, the Buck-Boost operates with peak, valley, and zero crossing current limits. The zero crossing limit is fixed at 0mA while the peak and valley limits are adjusted by the voltage loop if BBstIPAdptDis = 0.

In DCM mode, the valley current limit is negative so the end of phase 1 or 3 is determined by the zero-crossing current. In CCM mode, the valley current limit is ≥ 0mA if BBZCCmpEnb = 0. The end of phase 1 or 3 is thus determined by the valley current comparator.

Disabling the zero current crossing comparator reduces the Buck-Boost output ripple. Enabling the comparator improves EMI in CCM mode by removing the phase 4 stage in CCM mode that is otherwise present when BBZCCmpEnb = 1.

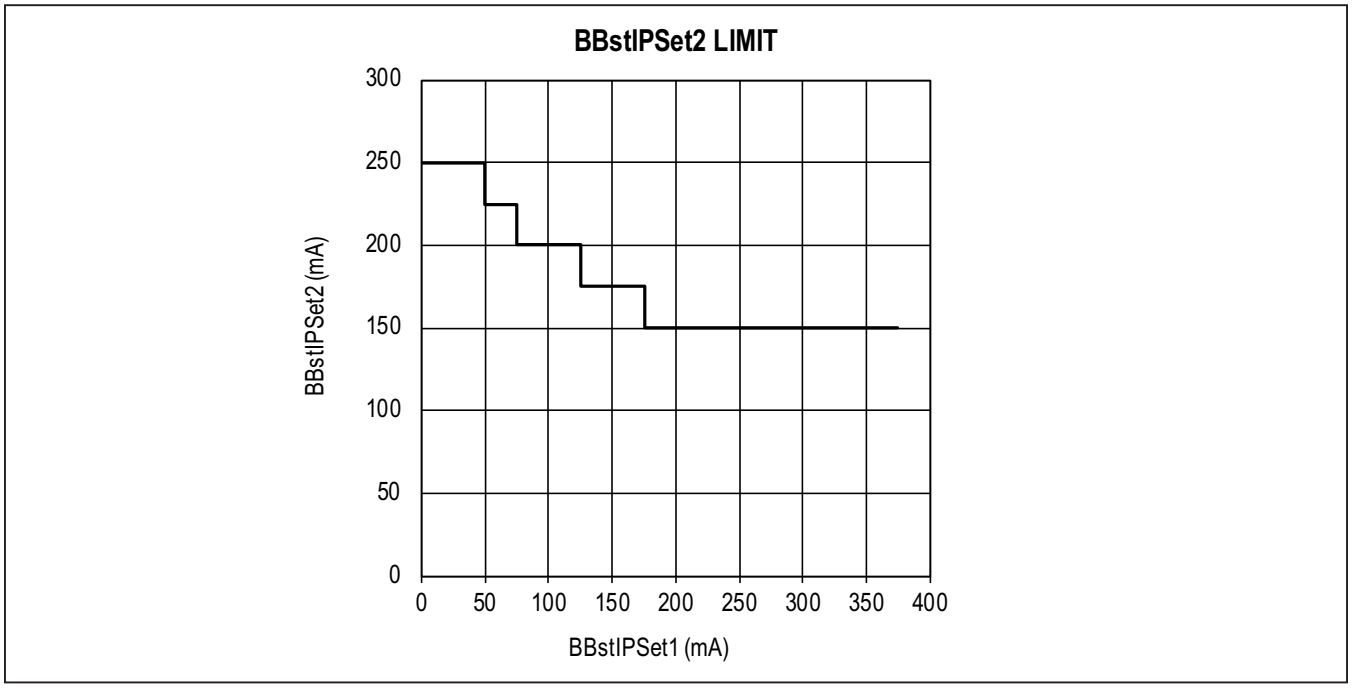


Figure 10. Recommended BBstIPSet1 and BBstIPSet2 Settings

Dynamic Voltage Scaling

All of the MAX20345's switching regulator outputs can be changed without restarting the regulator. This function is called dynamic voltage scaling (DVS). The MAX20345 provides three methods for dynamic voltage scaling of the bucks and Buck-Boost outputs: I²C DVS mode, GPIO DVS mode and SPI DVS Mode. The I²C mode is the slowest, but requires only simple I²C writes to execute. The GPIO control mode offers the fastest control and least complexity. The SPI mode offers a combination of speed and flexibility. Note that the slew-rate of the output voltage scaling is the same in all modes. Only the overhead and delay to initiate the transition changes. DVS modes are selected using the Buck_DVSCfg and BBstDVSCfg bitfields.

DVS Mode 0 (I²C DVS Mode)

DVS Mode 0 configures the regulator outputs to be controlled by I²C. If Buck_DVSCfg or BBstDVSCfg = 000, the output voltage of that regulator is controlled by I²C writes to the Buck_VSet or BBstVSet bitfield. Note, that a regulator in I²C mode must be unlocked before modifying the output voltage. Regulators are unlocked by setting their lock mask bit to 0 in LockMsk (register 0x52) and writing the unlock password 0x55 to the LockUnlock register (register 0x53).

DVS Mode 1 (GPIO DVS Mode)

In DVS Mode 1, two MPC inputs select the regulator output from four programmed values. To configure a regulator output for GPIO mode, set the corresponding Buck_DVSCfg or BBstDVSCfg bits to any value between 001 and 110. Each code selects a different pair of MPC pins to control the regulator. See the DVSCfg register descriptions for details on which MPC inputs are used for a code. In each case, the first MPC listed controls the low bit and the second MPC controls the high bit.

The four voltage levels share the same default value when the MAX20345 first powers on. After the startup process, each 6-bit output voltage level can be programmed using the I²C for each converter in the Buck_DVSVlt_ and BBstDVSVlt_ bitfields. As the MPC inputs change, the regulator output adjusts to the newly selected level as illustrated in Figure 11. Voltage levels are selected as shown in Table 2:

Table 2. DVS Mode 1 Voltage Selection

GPIO1	GPIO0	DVS VOLTAGE
0	0	Vlt0
0	1	Vlt1
1	0	Vlt2
1	1	Vlt3

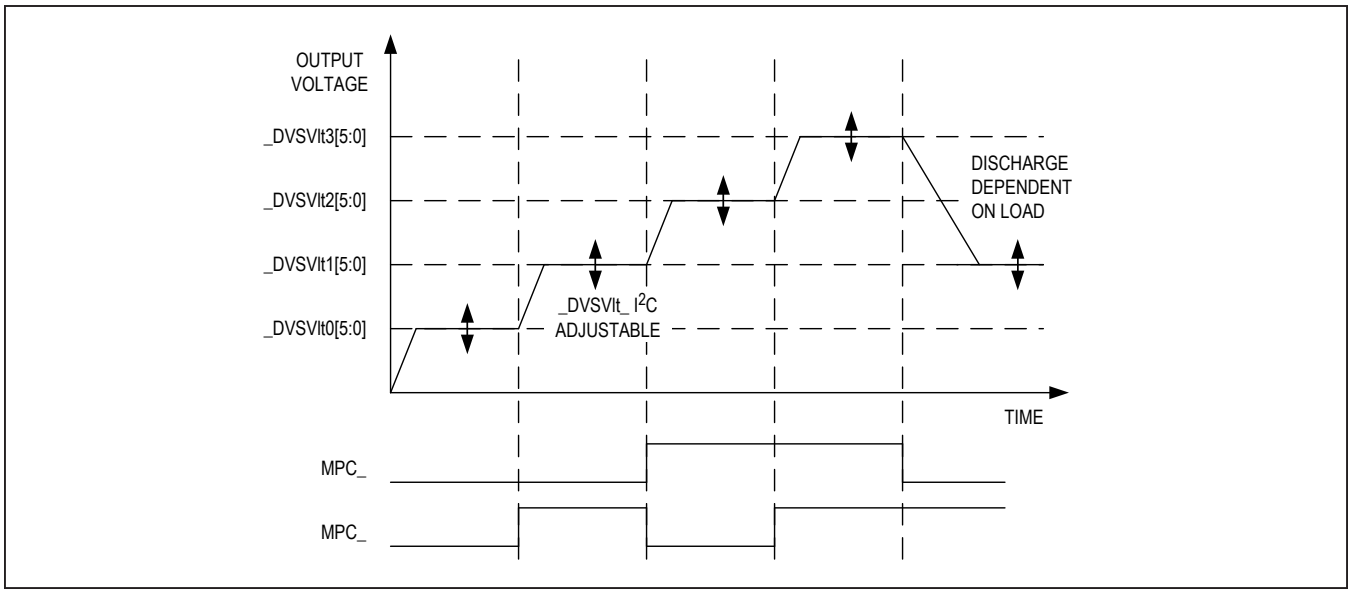


Figure 11. DVS Mode 1, GPIO Control

SPI DVS Mode (DVS Mode 2)

In DVS Mode 2, the regulator voltages are changed by writing command bytes to a 3-wire SPI interface. The SPI interface uses MPC0-2. MPC0 becomes the active-low chip select pin $\overline{CS}$, MPC1 becomes the clock SCLK, and MPC2 is the data input pin DIN. Data is clocked in on the SCLK rising edge. The maximum SPI clock frequency is 8MHz. A command byte comprises two address bits ADD[1:0] that select the regulator and six voltage bits VLT[5:0] that set the voltage. Figure 12 shows how data is clocked in SPI mode.

The output voltage is latched on the 8th rising edge of the clock. Note that voltages set by the SPI interface are mirrored in the Buck_VltSet and BBstVltSet bitfields for each converter. Figure 13 shows two regulators controlled in DVS Mode 2.

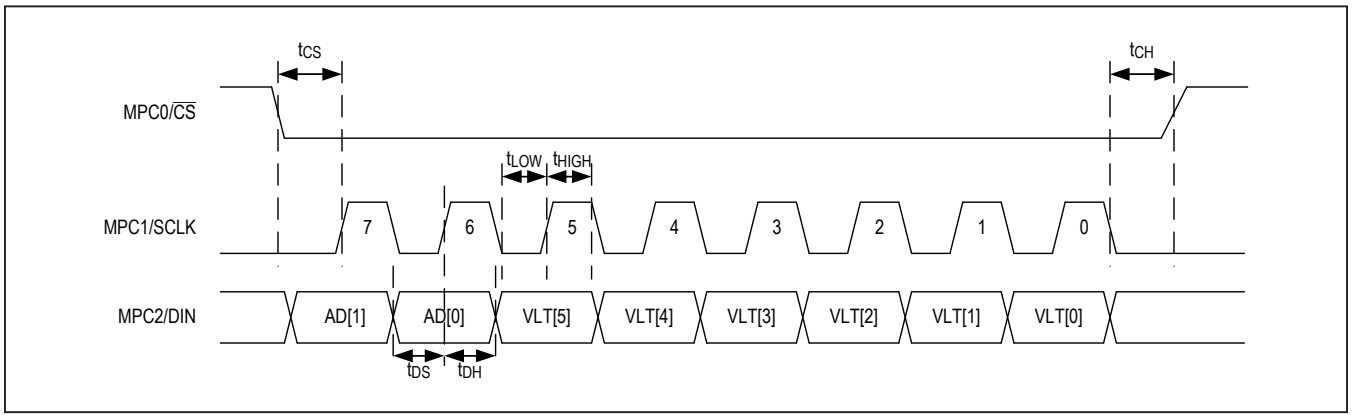


Figure 12. DVS Mode 2 SPI Timing

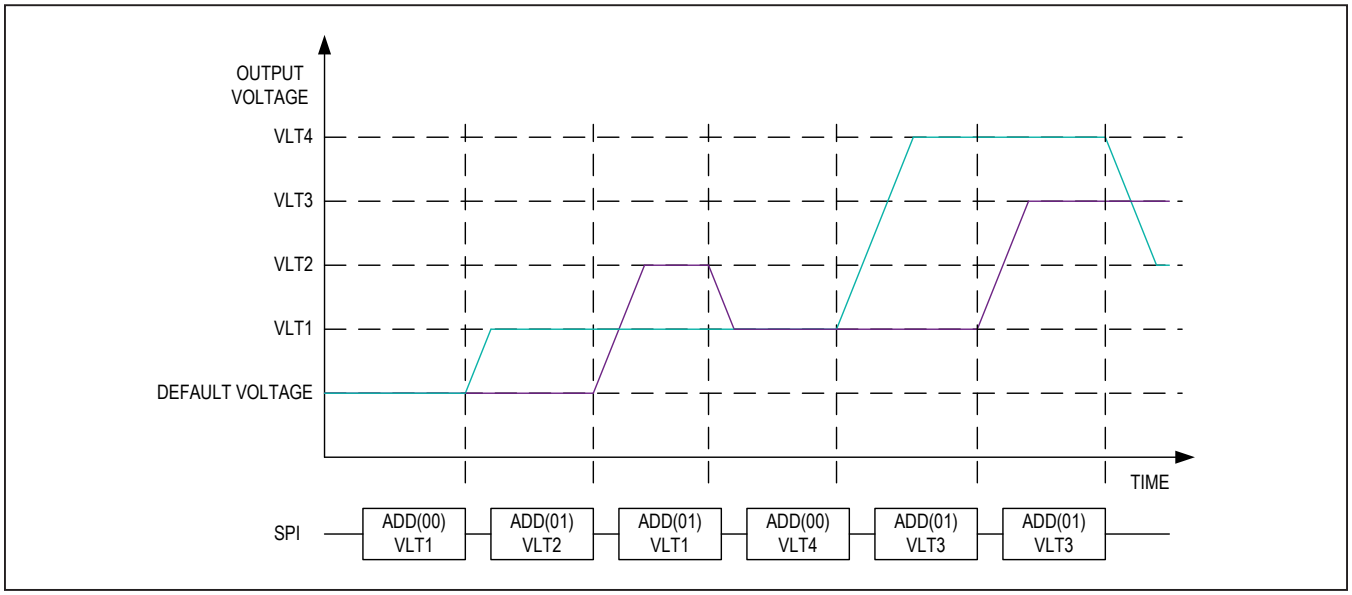


Figure 13. DVS Mode 2, SPI Control

The DVS SPI interface supports single and burst mode data transfer. In single-byte mode, $\overline{CS}$ goes high after each command byte is transferred. In burst-mode, all command bytes are written to the MAX20345 before $\overline{CS}$ returns high. Figure 14 shows how data is written in both modes.

I²C Interface Overview

The MAX20345 uses the two-wire I²C interface to communicate with a host microcontroller. The configuration settings and status information provided through this interface are detailed in the register descriptions. The device has the seven-bit slave address 0b0101000 (0x50 for writes, 0x51 for reads). Refer to the *Applications Information* section for details on the I²C interface.

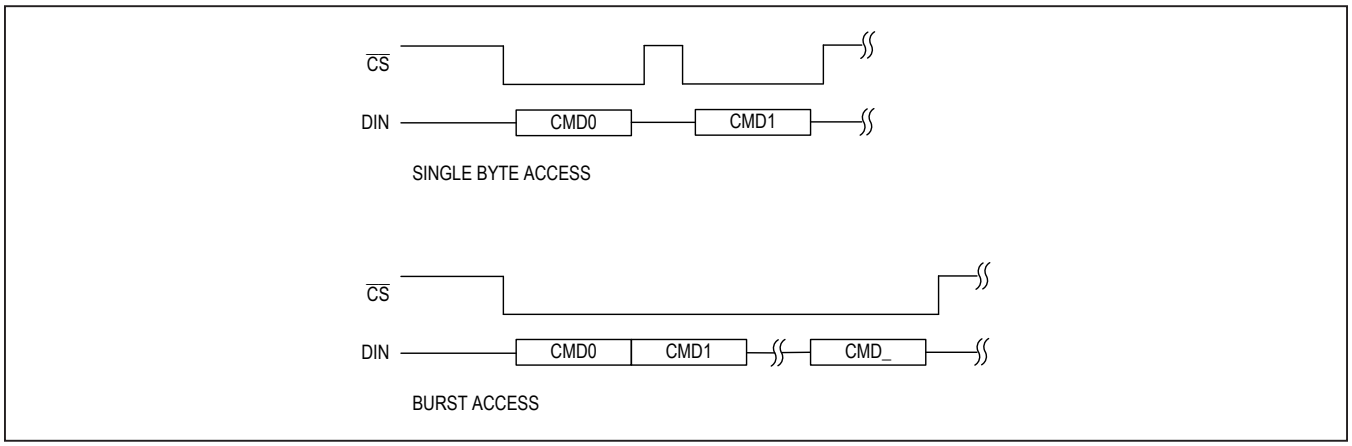


Figure 14. Single-Byte and Burst-Mode SPI Access

Register Map

ADDRESS	NAME	MSB							LSB
User									
0x00	ChipID[7:0]	ChipID[7:0]							
0x01	ChipRev[7:0]	ChipRev[7:0]							
0x02	Status0[7:0]	–	–	ThmStat[2:0]			ChgStat[2:0]		
0x03	Status1[7:0]	–	–	ILim	UsbOVP	UsbOk	ChgJEITA SD	ChgJEITA Reg	ChgTmo
0x04	Status2[7:0]	ThmSD	ThmtoMon	ThmLDO_ LSW	UVLOL DO2	–	–	–	–
0x05	Status3[7:0]	BBstFault	BBst UVLO	Sys BatLim	ChgSysLim	StepChg	ThmBk1	ThmBk2	ThmBk3
0x06	Int0[7:0]	Thm StatInt	ChgStatInt	ILimInt	UsbOVPInt	UsbOkInt	ChgJEITA SDInt	ChgJEITA RegInt	Chg TmoInt
0x07	Int1[7:0]	ThmSDInt	ThmtoMon Int	ThmLDO_ LSWInt	UVLOL DO2Int	–	–	LSW1 TmoInt	LSW2 TmoInt
0x08	Int2[7:0]	BBst FaultInt	BBst UVLOInt	SYSBat LimInt	ChgSys LimInt	Step ChgInt	Thm Bk1Int	Thm Bk2Int	Thm Bk3Int
0x09	IntMask0[7:0]	Thm StatIntM	Chg StatIntM	ILimIntM	Usb OVPIntM	Usb OkIntM	ChgJEITA SDIntM	ChgJEITA RegIntM	Chg TmoIntM
0x0A	IntMask1[7:0]	Thm SDIntM	ThmtoMon IntM	ThmLDO_ LSWIntM	UVLOL DO2IntM	–	–	LSW1 TmoIntM	LSW2 TmoIntM
0x0B	IntMask2[7:0]	BBstFau ltIntM	BBstUV LOIntM	SysBat LimIntM	ChgSys LimIntM	Step ChgIntM	Thm Bk1IntM	Thm Bk2IntM	Thm Bk3IntM
0x0C*	ILimCntl[7:0]	SysMin[2:0]			ILimBlank[1:0]		ILimCntl[2:0]		
0x0D*	ChgCntl0[7:0]	–	BatReChg[1:0]		BatReg[3:0]				ChgEn
0x0E*	ChgCntl1[7:0]	–	VPChg[2:0]			IPChg[1:0]		IChgDone[1:0]	
0x0F*	ChgTmr[7:0]	Chg AutoStp	ChgAuto ReSta	MtChgTmr[1:0]		FChgTmr[1:0]		PChgTmr[1:0]	
0x10*	StepChgCfg0[7:0]	–	ChgStepHyst[2:0]			ChgStepRise[3:0]			
0x11*	StepChgCfg1[7:0]	–	–	–	–	–	ChgIStep[2:0]		
0x12*	ThmCfg0[7:0]	ThmEn[2:0]			CoolBatReg[1:0]		CoolIFChg[2:0]		
0x13*	ThmCfg1[7:0]	–	–	–	RoomBatReg[1:0]		RoomIFChg[2:0]		
0x14*	ThmCfg2[7:0]	–	–	–	WarmBatReg[1:0]		WarmIFChg[2:0]		
0x15	MONCfg[7:0]	–	MONRatioCfg[1:0]		MonHiZ	MONCntl[3:0]			
0x16	Buck1Cfg[7:0]	Buck1Seq[2:0]			Buck1En[1:0]		Buck1IZCSet[1:0]		Buck1 PsvDsc
0x17	Buck1VSet[7:0]	Buck1 LowEMI	Buck1 RampEn	Buck1VSet[5:0]					
0x18	Buck1Set[7:0]	Buck1 IAdptEn	Buck1 SftStrt	Buck1 ActDsc	Buck1 FETScale	Buck1ISet[3:0]			
0x19	Buck1Ctr(0x19)	–	Buck1DVSCfg[2:0]			Buck1 MPC3	Buck1 MPC2	Buck1 MPC1	Buck1 MPC0
0x1A	Buck1 DVSCfg0[7:0]	–	–	Buck1DVSVlt0[5:0]					

**The register is reset to default value upon CHGIN rising/falling edge based on the UsbOkselect option. See Table 3 for the default UsbOkselect value.*

Register Map (continued)

ADDRESS	NAME	MSB							LSB
User									
0x1B	Buck1 DVSCfg1 [7:0]	–	–	Buck1DVSVlt1[5:0]					
0x1C	Buck1 DVSCfg2[7:0]	–	–	Buck1DVSVlt2[5:0]					
0x1D	Buck1 DVSCfg3[7:0]	–	–	Buck1DVSVlt3[5:0]					
0x1E	Buck1 DVSSPI[7:0]	–	–	Buck1SPIVlt[5:0]					
0x1F	Buck2Cfg[7:0]	Buck2Seq[2:0]			Buck2En[1:0]		Buck2IZCSet[1:0]		Buck2 PsvDsc
0x20	Buck2VSet[7:0]	Buck2 LowEMI	Buck2 RampEn	Buck2VSet[5:0]					
0x21	Buck2ISet[7:0]	Buck2 IAdptEn	Buck2 SftStrt	Buck2 ActDsc	Buck2 FETScale	Buck2ISet[3:0]			
0x22	Buck2Ctr[7:0]	–	Buck2DVSCfg[2:0]			Buck2 MPC3	Buck2 MPC2	Buck2 MPC1	Buck2 MPC0
0x23	Buck2 DVSCfg0[7:0]	–	–	Buck2DVSVlt0[5:0]					
0x24	Buck2 DVSCfg1[7:0]	–	–	Buck2DVSVlt1[5:0]					
0x25	Buck2 DVSCfg2[7:0]	–	–	Buck2DVSVlt2[5:0]					
0x26	Buck2 DVSCfg3[7:0]	–	–	Buck2DVSVlt3[5:0]					
0x27	Buck2 DVSSPI[7:0]	–	–	Buck2SPIVlt[5:0]					
0x28	Buck3Cfg[7:0]	Buck3Seq[2:0]			Buck3En[1:0]		Buck3IZCSet[1:0]		Buck3 PsvDsc
0x29	Buck3VSet[7:0]	Buck3 LowEMI	Buck3 RampEn	Buck3VSet[5:0]					
0x2A	Buck3ISet[7:0]	Buck3 IAdptEn	Buck3 SftStrt	Buck3 ActDsc	Buck3 FETScale	Buck3ISet[3:0]			
0x2B	Buck3Ctr[7:0]	–	Buck3DVSCfg[2:0]			Buck3 MPC3	Buck3 MPC2	Buck3 MPC1	Buck3 MPC0
0x2C	Buck3 DVSCfg0[7:0]	–	–	Buck3DVSVlt0[5:0]					
0x2D	Buck3 DVSCfg1[7:0]	–	–	Buck3DVSVlt1[5:0]					
0x2E	Buck3 DVSCfg2[7:0]	–	–	Buck3DVSVlt2[5:0]					
0x2F	Buck3 DVSCfg3[7:0]	–	–	Buck3DVSVlt3[5:0]					
0x30	Buck3 DVSSPI[7:0]	–	–	Buck3SPIVlt[5:0]					

Register Map (continued)

ADDRESS	NAME	MSB							LSB
User									
0x31	BBstCfg0[7:0]	BBstSeq[2:0]			BBstEn[1:0]		BBst RampEn	BBstMode	BBst PsvDsc
0x32	BBstVSet[7:0]	BBst LowEMI	BBstAct Dsc	BBstVSet[5:0]					
0x33	BBstISet[7:0]	BBstIPSet2[3:0]				BBstIPSet1[3:0]			
0x34	BBstCfg1[7:0]	BBstI PAdptDis	BBstFast	BBZC CmpDis	BBst FETScale	–	–	BBFHighSh[1:0]	
0x35	BBstCtr[7:0]	BBst MPC1FCT	BBstDVSCfg[2:0]			BBst MPC3	BBst MPC2	BBst MPC1	BBst MPC0
0x36	BBstDVSCfg0[7:0]	–	–	BBstDVSVlt0[5:0]					
0x37	BBstDVSCfg1[7:0]	–	–	BBstDVSVlt1[5:0]					
0x38	BBstDVSCfg2[7:0]	–	–	BBstDVSVlt2[5:0]					
0x39	BBstDVSCfg3[7:0]	–	–	BBstDVSVlt3[5:0]					
0x3A	BBstDVSSPI[7:0]	–	–	BBstSPIVlt[5:0]					
0x3B	LDO1Cfg[7:0]	LDO1Seq[2:0]			LDO1En[1:0]		LDO1 ActDsc	LDO1 Mode	LDO1 PsvDsc
0x3C	LDO1VSet[7:0]	–	–	–	LDO1VSet[4:0]				
0x3D	LDO1Ctr[7:0]	–	–	–	–	LDO1 MPC3	LDO1 MPC2	LDO1 MPC1	LDO1 MPC0
0x3E	LDO2Cfg[7:0]	LDO2Seq[2:0]			LDO2En[1:0]		LDO2 ActDsc	LDO2 Mode	LDO2 PsvDsc
0x3F	LDO2VSet[7:0]	–	–	–	LDO2VSet[4:0]				
0x40	LDO2Ctr[7:0]	–	–	–	–	LDO2 MPC3	LDO2 MPC2	LDO2 MPC1	LDO2 MPC0
0x41	LDO3Cfg[7:0]	LDO3Seq[2:0]			LDO3En[1:0]		LDO3 ActDsc	LDO3 Mode	LDO3 PsvDsc
0x42	LDO3VSet[7:0]	–	–	LDO3VSet[5:0]					
0x43	LDO3Ctr[7:0]	LDO3_MPC0CNT	LDO3_MPC0CNF	–	–	LDO3 MPC3	LDO3 MPC2	LDO3 MPC1	LDO3 MPC0
0x44	LSW1Cfg[7:0]	LSW1Seq[2:0]			LSW1En[1:0]		LSW1 ActDsc	LSW1 LowIq	LSW1 PsvDsc
0x45	LSW1Ctr[7:0]	–	–	–	–	LSW1 MPC3	LSW1 MPC2	LSW1 MPC1	LSW1 MPC0
0x46	LSW2Cfg[7:0]	LSW2Seq[2:0]			LSW2En[1:0]		LSW2 ActDsc	LSW2 LowIq	LSW2 PsvDsc
0x47	LSW2Ctr[7:0]	–	–	–	–	LSW2 MPC3	LSW2 MPC2	LSW2 MPC1	LSW2 MPC0
0x48	MPC0Cfg[7:0]	MPC0Pin	–	–	MPC0Out	MPC0OD	MPC0 HiZB	MPC0Res	MPC0Pup
0x49	MPC1Cfg[7:0]	MPC1Pin	–	–	MPC1Out	MPC1OD	MPC1 HiZB	MPC1Res	MPC1Pup

Register Map (continued)

ADDRESS	NAME	MSB							LSB
User									
0x4A	MPC2Cfg[7:0]	MPC2Pin	–	–	MPC2Out	MPC2OD	MPC2 HiZB	MPC2Res	MPC2Pup
0x4B	MPC3Cfg[7:0]	MPC3Pin	–	–	MPC3Out	MPC3OD	MPC3 HiZB	MPC3Res	MPC3Pup
0x4C	PFN[7:0]	–	–	–	–	–	–	PFN2Pin	PFN1Pin
0x4D	BootCfg[7:0]	PwrRstCfg[3:0]				SftRstCfg	BootDly[1:0]		Chg AlwTry
0x4E	PwrCfg[7:0]	ThmtoMon En	ThmtoMon Abr	–	–	–	–	–	StayOn
0x4F	PwrCmd[7:0]	PowerCommand[7:0]							
0x52	LockMsk[7:0]	LDO3Lck	LDO2Lck	LDO1Lck	BBstLck	Bk3Lck	Bk2Lck	Bk1Lck	ChgLck
0x53	LockUnlock[7:0]	PASSWORD[7:0]							

Register Descriptions

ChipID (0x00)

BIT	7	6	5	4	3	2	1	0
Field	ChipID[7:0]							
Reset	0x07							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ChipID	7:0	ChipID[7:0] indicates the version of MAX20345 in use.

ChipRev (0x01)

BIT	7	6	5	4	3	2	1	0
Field	ChipRev[7:0]							
Reset	0x02							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ChipRev	7:0	ChipRev[7:0] bits show information about the revision of the silicon in use.

Status0 (0x02)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ThmStat[2:0]			ChgStat[2:0]		
Reset	–	–	000			000		
Access Type	–	–	Read Only			Read Only		

BITFIELD	BITS	DESCRIPTION
ThmStat	5:3	Status of Thermistor Monitoring 000 = Cold Temperature Region 001 = Cool Temperature Region 010 = Room Temperature Region 011 = Warm Temperature Region 100 = Hot Temperature Region 101 = No thermistor detected (THM high due to external pullup). Note that if a parallel resistor is used for thermistor monitoring, this status may not function properly. 110 = NTC input disable by ThmEn[2:0] 111 = Detection disabled because CHGIN is not present. THM can still be measured by IVMON.
ChgStat	2:0	Status of Charger Mode 000 = Charger off 001 = Charging suspended due to temperature (see Figure 4) 010 = Pre-charge in progress 011 = Fast-charge constant current mode in progress 100 = Fast-charge constant voltage mode in progress 101 = Maintain charge in progress 110 = Maintain charge timer done 111 = Charger fault condition (see Figure 4)

Status1 (0x03)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ILim	UsbOVP	UsbOk	ChgJEITASD	ChgJEITAReg	ChgTmo
Reset	–	–	0	0	0	0	0	0
Access Type	–	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
ILim	5	Status of CHGIN Input Current Limit 0 = CHGIN input current below limit 1 = CHGIN input current limit active
UsbOVP	4	Status of CHGIN OVP 0 = CHGIN overvoltage not detected 1 = CHGIN overvoltage detected
UsbOk	3	Status of CHGIN Input 0 = CHGIN Input not present or outside of valid range 1 = CHGIN Input present and valid
ChgJEITASD	2	Status of JEITA Thermal Shutdown 0 = Charger in normal operating mode, or disabled 1 = Charger is in thermal shutdown as set by ThmEn[2:0]
ChgJEITAReg	1	Status of Thermal Regulation 0 = Charger is in normal operating mode, or disabled 1 = Charger is in thermal regulation mode and charging current is being actively reduced according to JEITA settings
ChgTmo	0	Status of Charger Time-Out Condition 0 = Charger is in normal operating mode, or disabled 1 = Charger has reached a time-out condition

Status2 (0x04)

BIT	7	6	5	4	3	2	1	0
Field	ThmSD	ThmtoMon	ThmLDO_LSW	UVLOLDO2	–	–	–	–
Reset	0		0	0	–	–	–	–
Access Type	Read Only	Read Only	Read Only	Read Only	–	–	–	–

BITFIELD	BITS	DESCRIPTION
ThmSD	7	Status of Charger and Limiter Thermal Shutdown 0 = Charger and Limiter operating normally 1 = Charger and Limiter in thermal shutdown
ThmtoMon	6	Status of the One-Shot THM Monitor 0 = MON MUX under manual control 1 = MON MUX performing one-shot THM measurement
ThmLDO_LSW	5	Status of LDO1, LDO2, LDO3, LSW1, LSW2 Thermal Shutdown 0 = All the above blocks are operating normally 1 = One of the above blocks is in thermal shutdown.
UVLOLDO2	4	Status of LDO2 UVLO 0 = LDO2 operating normally 1 = LDO2 UVLO active

Status3 (0x05)

BIT	7	6	5	4	3	2	1	0
Field	BBstFault	BBstUVLO	SysBatLim	ChgSysLim	StepChg	ThmBk1	ThmBk2	ThmBk3
Reset			0	0	0	0	0	0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
BBstFault	7	Status of Buck-Boost Fault 0 = Buck-Boost operating normally 1 = Buck-Boost under fault condition
BBstUVLO	6	Status of Buck-Boost UVLO 0 = Buck-Boost operating normally 1 = Buck-Boost UVLO active
SysBatLim	5	Status of SYS Regulation Current Limit 0 = Charge current is not being actively reduced to regulate SYS collapse 1 = Charge current actively being reduced to regulate SYS collapse
ChgSysLim	4	Status of CHGIN Regulation Current Limit 0 = Input current limit normal 1 = Input current limit being reduced to regulate CHGIN collapse
StepChg	3	Status of Charger Step Charge 0 = Charger is not in step-charging mode 1 = Charger is in step-charging mode (fast-charge current reduction)
ThmBk1	2	Status of Buck1 Thermal Shutdown 0 = Buck1 operating normally 1 = Buck1 in thermal shutdown
ThmBk2	1	Status of Buck2 Thermal Shutdown 0 = Buck2 operating normally 1 = Buck2 in thermal shutdown
ThmBk3	0	Status of Buck3 Thermal Shutdown 0 = Buck3 operating normally 1 = Buck3 in thermal shutdown

Int0 (0x06)

BIT	7	6	5	4	3	2	1	0
Field	ThmStatInt	ChgStatInt	ILimInt	UsbOVPInt	UsbOkInt	ChgJEITA SDInt	ChgJEITA RegInt	ChgTmoInt
Reset	0	0	0	0	0	0	0	0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
ThmStatInt	7	Change in ThmStat caused an interrupt
ChgStatInt	6	Change in ChgStat caused an interrupt
ILimInt	5	Input current limit caused an interrupt
UsbOVPInt	4	Change in UsbOVP caused an interrupt
UsbOkInt	3	Change in UsbOk caused an interrupt
ChgJEITASDInt	2	Change in ChgJEITASD caused an interrupt
ChgJEITARegInt	1	Change in ChgJEITAReg caused an interrupt
ChgTmoInt	0	Change in ChgTmo caused an interrupt

Int1 (0x07)

BIT	7	6	5	4	3	2	1	0
Field	ThmSDInt	ThmtoMonInt	ThmLDO_ LSWInt	UVLOL DO2Int	–	–	LSW1 TmoInt	LSW2 TmoInt
Reset	0		0	0	–	–	0	0
Access Type	Read Clears All	Read Only	Read Clears All	Read Clears All	–	–	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
ThmSDInt	7	Change in ThmSD caused an interrupt
ThmtoMonInt	6	Change in ThmtoMon caused an interrupt
ThmLDO_LSWInt	5	Change in ThmLDO_LSW caused an interrupt
UVLOLDO2Int	4	Change in UVLOLDO2 caused an interrupt
LSW1TmoInt	1	LSW1 failed to startup during timeout period
LSW2TmoInt	0	LSW2 failed to startup during timeout period

Int2 (0x08)

BIT	7	6	5	4	3	2	1	0
Field	BBstFaultInt	BBstU VLOInt	SYSBat LimInt	ChgSys LimInt	StepChgInt	ThmBk1Int	ThmBk2Int	ThmBk3Int
Reset			0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
BBstFaultInt	7	Change in BBstFault caused an interrupt
BBstUVLOInt	6	Change in BBstUVLO caused an interrupt
SYSBatLimInt	5	Change in SysBatLim caused an interrupt
ChgSysLimInt	4	Change in ChgSysLim caused an interrupt
StepChgInt	3	Change in StepChg caused an interrupt
ThmBk1Int	2	Change in ThmBk1 caused an interrupt
ThmBk2Int	1	Change in ThmBk2 caused an interrupt
ThmBk3Int	0	Change in ThmBk3 caused an interrupt

IntMask0 (0x09)

BIT	7	6	5	4	3	2	1	0
Field	Thm StatIntM	ChgStatIntM	ILimIntM	Usb OVPIntM	UsbOkIntM	ChgJEITAS DIntM	ChgJEITA RegIntM	Chg TmoIntM
Reset	0	0	0	0	0	0	0	0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
ThmStatIntM	7	ThmStatIntM masks the ThmStatInt interrupt in the Int0 register (0x06). 0 = Masked 1 = Not masked
ChgStatIntM	6	ChgStatIntM masks the ChgStatInt interrupt in the Int0 register (0x06). 0 = Masked 1 = Not masked
ILimIntM	5	ILimIntM masks the ILimInt interrupt in the Int0 register (0x06). 0 = Masked 1 = Not masked
UsbOVPIntM	4	UsbOVPIntM masks the UsbOVPInt interrupt in the Int0 register (0x06). 0 = Masked 1 = Not masked
UsbOkIntM	3	UsbOkIntM masks the UsbOkInt interrupt in the Int0 register (0x06). 0 = Masked 1 = Not masked
ChgJEITASDIntM	2	ChgThmSDIntM masks the ChgThmSDInt interrupt in the Int0 register (0x06). 0 = Masked 1 = Not masked
ChgJEITARegIntM	1	ChgJEITARegIntM masks the ChgJEITARegInt interrupt in the Int0 register (0x06). 0 = Masked 1 = Not masked
ChgTmoIntM	0	ChgTmoIntM masks the ChgTmoInt interrupt in the Int0 register (0x06). 0 = Masked 1 = Not masked

IntMask1 (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	ThmSDIntM	Thmto MonIntM	ThmLDO_ LSWIntM	UVLOL DO2IntM	–	–	LSW1T moIntM	LSW2T moIntM
Reset	0		0	0	–	–	0	0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
ThmSDIntM	7	ThmSDIntM masks the ThmSDInt interrupt in the Int1 register (0x07). 0 = Masked 1 = Not masked
ThmtoMonIntM	6	ThmtoMonIntM masks the ThmtoMonInt interrupt in the Int1 register (0x07). 0 = Masked 1 = Not masked
ThmLDO_LSWIntM	5	ThmLDO_LSWIntM masks the ThmLDO_LSWInt interrupt in the Int1 register (0x07). 0 = Masked 1 = Not masked
UVLOLDO2IntM	4	UVLOLDO2IntM masks the UVLOLDO2Int interrupt in the Int1 register (0x07). 0 = Masked 1 = Not masked
LSW1TmoIntM	1	LSW1TmoIntM masks the LSW1TmoInt interrupt in the Int1 register (0x07). 0 = Masked 1 = Not masked
LSW2TmoIntM	0	LSW2TmoIntM masks the LSW2TmoInt interrupt in the Int1 register (0x07). 0 = Masked 1 = Not masked

IntMask2 (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SysBatLimIntM	ChgSysLimIntM	StepChgIntM	ThmBk1IntM	ThmBk2IntM	ThmBk3IntM
Reset	–	–	0	0	0	0	0	0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
SysBatLimIntM	5	SysBatLimIntM masks the SysBatLimInt interrupt in the Int2 register (0x08). 0 = Masked 1 = Not masked
ChgSysLimIntM	4	ChgSysLimIntM masks the ChgSysLimInt interrupt in the Int2 register (0x08). 0 = Masked 1 = Not masked
StepChgIntM	3	StepChgIntM masks the StepChgInt interrupt in the Int2 register (0x08). 0 = Masked 1 = Not masked
ThmBk1IntM	2	ThmBk1IntM masks the ThmBk1Int interrupt in the Int2 register (0x08). 0 = Masked 1 = Not masked
ThmBk2IntM	1	ThmBk2IntM masks the ThmBk2Int interrupt in the Int2 register (0x08). 0 = Masked 1 = Not masked
ThmBk3IntM	0	ThmBk3IntM masks the ThmBk3Int interrupt in the Int2 register (0x08). 0 = Masked 1 = Not masked

ILimCntl (0x0C)*

BIT	7	6	5	4	3	2	1	0
Field	SysMin[2:0]			ILimBlank[1:0]		ILimCntl[2:0]		
Reset								
Access Type	Write, Read			Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION
SysMin	7:5	System Voltage Minimum Threshold Voltage below which charging current is reduced to prevent SYS from collapsing 000 = 3.6V 001 = 3.7V 010 = 3.8V 011 = 3.9V 100 = 4.0V 101 = 4.1V 110 = 4.2V 111 = 4.3V
ILimBlank	4:3	CHGIN Current Limiter Blanking Time 00 = No debounce (allow a few clock cycles for resampling) 01 = 0.5ms 10 = 1ms 11 = 10ms
ILimCntl	2:0	CHGIN Programmable Input Current Limit 000 = 50mA 001 = 90mA 010 = 150mA 011 = 200mA 100 = 300mA 101 = 400mA 110 = 450mA 111 = 1000mA

**The register is reset to default value upon CHGIN rising/falling edge based on the UsbOkselect option. See Table 3 for the default UsbOkselect value.*

ChgCntl0 (0x0D)*

BIT	7	6	5	4	3	2	1	0
Field	–	BatReChg[1:0]		BatReg[3:0]				ChgEn
Reset	–							
Access Type	–	Write, Read		Write, Read				Write, Read

BITFIELD	BITS	DESCRIPTION
BatReChg	6:5	Recharge Threshold in Relation to BatReg[3:0] 00 = BatReg - 70mV 01 = BatReg - 120mV 10 = BatReg - 170mV 11 = BatReg - 220mV
BatReg	4:1	Battery Regulation Voltage 0000 = 4.05V 0001 = 4.10V 0010 = 4.15V 0011 = 4.20V 0100 = 4.25V 0101 = 4.30V 0110 = 4.35V 0111 = 4.40V 1000 = 4.45V 1001 = 4.50V 1010 = 4.55V 1011 = 4.60V
ChgEn	0	On/Off Control for Charger Does not affect SYS node 0 = Charger Disabled 1 = Charger Enabled

**The register is reset to default value upon CHGIN rising/falling edge based on the UsbOkselect option (see Table 3 for the default UsbOkselect value).*

ChgCntl1 (0x0E)*

BIT	7	6	5	4	3	2	1	0
Field	–	VPChg[2:0]			IPChg[1:0]		IChgDone[1:0]	
Reset	–							
Access Type	–	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
VPChg	6:4	Precharge Voltage Threshold Setting 000 = 2.10V 001 = 2.25V 010 = 2.40V 011 = 2.55V 100 = 2.70V 101 = 2.85V 110 = 3.00V 111 = 3.15V
IPChg	3:2	Precharge Current Setting 00 = 0.05 x I_{FCHG} 01 = 0.1 x I_{FCHG} 10 = 0.2 x I_{FCHG} 11 = 0.3 x I_{FCHG}
IChgDone	1:0	Charge Done Current Threshold Setting 00 = 0.05 x I_{FCHG} 01 = 0.1 x I_{FCHG} 10 = 0.2 x I_{FCHG} 11 = 0.3 x I_{FCHG}

**The register is reset to default value upon CHGIN rising/falling edge based on the UsbOkselect option. See Table 3 for the default UsbOkselect value).*

ChgTmr (0x0F)*

BIT	7	6	5	4	3	2	1	0
Field	ChgAutoStp	ChgAutoReSta	MtChgTmr[1:0]		FChgTmr[1:0]		PChgTmr[1:0]	
Reset								
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
ChgAutoStp	7	Charger Auto-Stop Controls the Transition from Maintain Charge to Maintain Charge Done. See Figure 4. 0 = Auto-Stop Disabled 1 = Auto-Stop Enabled
ChgAutoReSta	6	Charger Auto-Restart Control See Figure 4. 0 = Charger Remains in Maintain Charge Done even when V_{BAT} is Less than Charger Restart Threshold 1 = Charger Automatically Restarts when V_{BAT} Drops Below Charger Restart Threshold
MtChgTmr	5:4	Maintain Charge Timer Setting 00 = 0min 01 = 15min 10 = 30min 11 = 60min
FChgTmr	3:2	Fast Charge Timer Setting 00 = 75min 01 = 150min 10 = 300min 11 = 600min
PChgTmr	1:0	Precharge Timer Setting 00 = 30min 01 = 60min 10 = 120min 11 = 240min

**The register is reset to default value upon CHGIN rising/falling edge based on the UsbOkselect option. See Table 3 for the default UsbOkselect value.*

StepChgCfg0 (0x10)*

BIT	7	6	5	4	3	2	1	0
Field	–	ChgStepHyst[2:0]			ChgStepRise[3:0]			
Reset	–							
Access Type	–	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
ChgStepHyst	6:4	Step Charge Voltage Threshold Hysteresis 000 = 100mV 001 = 200mV 010 = 300mV 011 = 400mV 100 = 500mV 101 = 600mV 11x = Reserved
ChgStepRise	3:0	Step Charge Voltage Threshold 0000 = 3.80V 0001 = 3.85V 0010 = 3.90V 0011 = 3.95V 0100 = 4.00V 0101 = 4.05V 0110 = 4.10V 0111 = 4.15V 1000 = 4.20V 1001 = 4.25V 1010 = 4.30V 1011 = 4.35V 1100 = 4.40V 1101 = 4.45V 1110 = 4.50V 1111 = 4.55V

**The register is reset to default value upon CHGIN rising/falling edge based on the UsbOkselect option (see Table 3 for the default UsbOkselect value).*

StepChgCfg1 (0x11)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	ChgIStep[2:0]		
Reset	–	–	–	–	–			
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
ChgIStep	2:0	Step Charge Current Scaling Sets the modified Fast Charge current once the Step Charge Threshold is exceeded. The Fast Charge current is the minimum of the value set by ChgIStep and the applicable JEITA current scaling register (0x12, 0x13, or 0x14). 000 = 0.2 x I_{FCHG} 001 = 0.3 x I_{FCHG} 010 = 0.4 x I_{FCHG} 011 = 0.5 x I_{FCHG} 100 = 0.6 x I_{FCHG} 101 = 0.7 x I_{FCHG} 110 = 0.8 x I_{FCHG} 111 = 1.0 x I_{FCHG}

ThmCfg0 (0x12)*

BIT	7	6	5	4	3	2	1	0
Field	ThmEn[2:0]			CoolBatReg[1:0]		CoolIFChg[2:0]		
Reset				11		111		
Access Type	Write, Read			Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION
ThmEn	7:5	Charger Thermal Monitor Control 000 = Thermal monitoring disabled 001 = Charging enabled in the cool and room temperature regions 010 = Charging enabled in the room and warm temperature regions 011 = Charging enabled in the cool, room and warm temperature regions 1xx = Reserved
CoolBatReg	4:3	Cool Zone Battery Regulation Voltage Sets the modified BatReg[3:0] in the Cool Temperature Zone 00 = BatReg - 150mV 01 = BatReg -100mV 10 = BatReg - 50mV 11 = BatReg
CoolIFChg	2:0	Cool Zone Fast Charge Current Scaling Sets the modified Fast Charge current in the Cool Temperature Zone 000 = 0.2 x I_{FCHG} 001 = 0.3 x I_{FCHG} 010 = 0.4 x I_{FCHG} 011 = 0.5 x I_{FCHG} 100 = 0.6 x I_{FCHG} 101 = 0.7 x I_{FCHG} 110 = 0.8 x I_{FCHG} 111 = 1.0 x I_{FCHG}

**The register is reset to default value upon CHGIN rising/falling edge based on the UsbOkselect option (see Table 3 for the default UsbOkselect value).*

ThmCfg1 (0x13)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	RoomBatReg[1:0]		RoomIFChg[2:0]		
Reset	–	–	–	11		111		
Access Type	–	–	–	Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION
RoomBatReg	4:3	Room Zone Battery Regulation Voltage Sets the modified BatReg[3:0] in the Room Temperature Zone 00 = BatReg - 150mV 01 = BatReg -100mV 10 = BatReg - 50mV 11 = BatReg
RoomIFChg	2:0	Room Zone Fast Charge Current Scaling Sets the modified Fast Charge current in the Room Temperature Zone 000 = 0.2 x I_{FCHG} 001 = 0.3 x I_{FCHG} 010 = 0.4 x I_{FCHG} 011 = 0.5 x I_{FCHG} 100 = 0.6 x I_{FCHG} 101 = 0.7 x I_{FCHG} 110 = 0.8 x I_{FCHG} 111 = 1.0 x I_{FCHG}

ThmCfg2 (0x14)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	WarmBatReg[1:0]		WarmIFChg[2:0]		
Reset	–	–	–	11		111		
Access Type	–	–	–	Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION
WarmBatReg	4:3	Warm Zone Battery Regulation Voltage Sets the modified BatReg[3:0] in the Warm Temperature Zone 00 = BatReg - 150mV 01 = BatReg -100mV 10 = BatReg - 50mV 11 = BatReg
WarmIFChg	2:0	Warm Zone Fast Charge Current Scaling Sets Modified Fast Charge Current in the Warm Temperature Zone 000 = 0.2 x I_{FCHG} 001 = 0.3 x I_{FCHG} 010 = 0.4 x I_{FCHG} 011 = 0.5 x I_{FCHG} 100 = 0.6 x I_{FCHG} 101 = 0.7 x I_{FCHG} 110 = 0.8 x I_{FCHG} 111 = 1.0 x I_{FCHG}

**The register is reset to default value upon CHGIN rising/falling edge based on the UsbOkselect option. See Table 3 for the default UsbOkselect value).*

MONCfg (0x15)

BIT	7	6	5	4	3	2	1	0
Field	–	MONRatioCfg[1:0]		MonHiZ	MONCntl[3:0]			
Reset	–	00		1	0000			
Access Type	–	Write, Read		Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION
MONRatioCfg	6:5	IVMON Resistive Partition Selector 00 = 1:1 01 = 2:1 10 = 3:1 11 = 4:1
MonHiZ	4	IVMON Pin Off Mode Condition 0 = Pulled Low by 59kΩ (typ) pulldown resistor 1 = Hi-Z
MONCntl	3:0	IVMON Multiplexer Input Source Selection 0000 = Off Mode 0001 = Charger Current (buffered version of V_{ISET}) 0010 = BAT 0011 = SYS 0100 = BK1OUT 0101 = BK2OUT 0110 = BK3OUT 0111 = L1OUT 1000 = L2OUT 1001 = L3OUT 1010 = BBOUT 1011 = THM 1100 = TPU 1101 = Reserved 111x = Reserved

Buck1Cfg (0x16)

BIT	7	6	5	4	3	2	1	0
Field	Buck1Seq[2:0]			Buck1En[1:0]		Buck1IZCSet[1:0]		Buck1PsvDsc
Reset								1
Access Type	Read Only			Write, Read		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION
Buck1Seq	7:5	Buck1 Enable Configuration 000 = Disabled 001 = Reserved 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Reserved 110 = Reserved 111 = Controlled by Buck1En [1:0] after 100% of Boot/POR Process Delay Control
Buck1En	4:3	Buck1 Enable Configuration (effective only when Buck1Seq = 111) 00 = Disabled: BK1OUT not actively discharged unless Hard-Reset/Shut-down/Off mode 01 = Enabled 10 = Controlled by MPC_ (See Buck1MPC_ bits in register 0x19) 11 = Reserved
Buck1IZCSet	2:1	Buck1 Zero Crossing Current Threshold Optimizes Buck1 for a given voltage setting. 00 = 10mA, Use for Buck1VSet < 1V 01 = 20mA, Use for 1V ≤ Buck1VSet < 1.8V 10 = 30mA, Use for 1.8V ≤ Buck1VSet < 3V 11 = 40mA, Use for Buck1Vset ≥ 3V
Buck1PsvDsc	0	Buck1 Passive Discharge Control 0 = Buck1 passively discharged only in Hard-Reset 1 = Buck1 passively discharged in Hard-Reset or Enable Low

Buck1VSet (0x17)

BIT	7	6	5	4	3	2	1	0
Field	Buck1LowEMI	Buck1RampEn	Buck1VSet[5:0]					
Reset	0	1						
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck1LowEMI	7	Buck1 Low EMI Mode 0 = Normal operation 1 = Increase rise/fall time on BK1LX by 3x
Buck1RampEn	6	Buck1 Ramp Enable 0 = Voltage setting transition is performed without intermediate steps 1 = Voltage setting transition to a higher value is performed with incremental steps every 20µs
Buck1VSet	5:0	Buck1 Output Voltage Setting 0.7V to (63 x Bk1Step), linear scale, increments of Bk1Step. See Table 3, e.g., for Bk1Step = 10mV: 000000 = 0.7V 000001 = 0.71V … 111111 = 1.33V

Buck1ISet (0x18)

BIT	7	6	5	4	3	2	1	0
Field	Buck1IAdptEn	Buck1SftStrt	Buck1ActDsc	Buck1FETScale	Buck1ISet[3:0]			
Reset	1		0					
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION
Buck1IAdptEn	7	Buck1 Adaptive Peak Current Mode 0 = Inductor peak current fixed at the programmed value by means of Buck1ISet 1 = Inductor peak current automatically increased to provide better load regulation
Buck1SftStrt	6	Buck1 Soft-Start Time Buck1 has reduced current capability during soft-start 0 = 50ms 1 = 5ms
Buck1ActDsc	5	Buck1 Active Discharge Control 0 = Buck1 actively discharged only in Hard-Reset 1 = Buck1 actively discharged in Hard-Reset or Enable Low
Buck1FETScale	4	Buck1 Force FET Scaling Reduce the FET size by a factor of two. Used to optimize the efficiency when Buck1ISet must be < 100mA (e.g., to mitigate noise at low frequencies). 0 = FET scaling disabled 1 = FET scaling enabled
Buck1ISet	3:0	Buck1 Inductor Peak Current Setting For the best efficiency, use = between 150mA and 200mA. Linear scale, 25mA increments, settings below 75mA can be limited by the minimum t_{ON} 0000 = 0mA 0001 = 25mA ... 1111 = 375mA

Buck1Ctr (0x19)

BIT	7	6	5	4	3	2	1	0
Field	–	Buck1DVSCfg[2:0]			Buck1MPC3	Buck1MPC2	Buck1MPC1	Buck1MPC0
Reset	–	000			0	0	0	1
Access Type	–	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
Buck1DVSCfg	6:4	Buck1 DVS Configuration 000 = Disabled 001 = DVS Mode 1 Enabled, Buck1 DVS controlled by MPC0 and MPC1 010 = DVS Mode 1 Enabled, Buck1 DVS controlled by MPC0 and MPC2 011 = DVS Mode 1 Enabled, Buck1 DVS controlled by MPC0 and MPC3 100 = DVS Mode 1 Enabled, Buck1 DVS controlled by MPC1 and MPC2 101 = DVS Mode 1 Enabled, Buck1 DVS controlled by MPC1 and MPC3 110 = DVS Mode 1 Enabled, Buck1 DVS controlled by MPC2 and MPC3 111 = DVS Mode 2 Enabled (SPI: MPC0 is $\overline{CS}$, MPC1 is SCLK, MPC2 is DIN.)
Buck1MPC3	3	Buck1 MPC3 Enable Control Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs. 0 = MPC3 does not control Buck1 1 = Buck1 controlled by MPC3
Buck1MPC2	2	Buck1 MPC2 Enable Control Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs. 0 = MPC2 does not control Buck1 1 = Buck1 controlled by MPC2
Buck1MPC1	1	Buck1 MPC1 Enable Control Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs. 0 = MPC1 does not control Buck1 1 = Buck1 controlled by MPC1
Buck1MPC0	0	Buck1 MPC0 Enable Control Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs. 0 = MPC0 does not control Buck1 1 = Buck1 controlled by MPC0

Buck1DVSCfg0 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck1DVSVlt0[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck1DVSVlt0	5:0	Buck1 Alternate Output Voltage Setting 1 (Controlling MPCs = 00) 0.7V to (63 x Bk1Step), linear scale, increments of Bk1Step. See Table 3, e.g., for Bk1Step = 10mV: 000000 = 0.7V 000001 = 0.71V … 111111 = 1.33V

Buck1DVSCfg1 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck1DVSVlt1[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck1DVSVlt1	5:0	Buck1 Alternate Output Voltage Setting 2 (Controlling MPCs = 01) 0.7V to (63 x Bk1Step), linear scale, increments of Bk1Step. See Table 3, e.g., for Bk1Step = 10mV: 000000 = 0.7V 000001 = 0.71V … 111111 = 1.33V

Buck1DVSCfg2 (0x1C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck1DVSVlt2[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck1DVSVlt2	5:0	Buck1 Alternate Output Voltage Setting 1 (Controlling MPCs = 10) 0.7V to (63 x Bk1Step), linear scale, increments of Bk1Step. See Table 3, e.g., for Bk1Step = 10mV: 000000 = 0.7V 000001 = 0.71V … 111111 = 1.33V

Buck1DVSCfg3 (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck1DVSVlt3[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck1DVSVlt3	5:0	Buck1 Alternate Output Voltage Setting 1 (Controlling MPCs = 11) 0.7V to (63 x Bk1Step), linear scale, increments of Bk1Step. See Table 3, e.g., for Bk1Step = 10mV: 000000 = 0.7V 000001 = 0.71V … 111111 = 1.33V

Buck1DVSSPI (0x1E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck1SPIVlt[5:0]					
Reset	–	–						
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
Buck1SPIVlt	5:0	Buck1 SPI DVS Readback 0.7V to (63 x Bk1Step), linear scale, increments of Bk1Step. See Table 3, e.g., for Bk1Step = 10mV: 000000 = 0.7V 000001 = 0.71V … 111111 = 1.33V

Buck2Cfg (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	Buck2Seq[2:0]			Buck2En[1:0]		Buck2IZCSet[1:0]		Buck2PsvDsc
Reset								0b1
Access Type	Read Only			Write, Read		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION
Buck2Seq	7:5	Buck2 Enable Configuration 000 = Disabled 001 = Reserved 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Reserved 110 = Reserved 111 = Controlled by Buck2En [1:0] after 100% of Boot/POR Process Delay Control
Buck2En	4:3	Buck2 Enable Configuration (effective only when Buck2Seq = 111) 00 = Disabled: BK2OUT not actively discharged unless Hard-Reset/Shut-down/Off mode 01 = Enabled 10 = Controlled by MPC_ (See Buck2MPC_ bits in register 0x22) 11 = Reserved
Buck2IZCSet	2:1	Buck2 Zero Crossing Current Threshold Optimizes Buck2 for a given voltage setting. 00 = 10mA, Use for Buck2VSet < 1V 01 = 20mA, Use for 1V ≤ Buck2VSet < 1.8V 10 = 30mA, Use for 1.8V ≤ Buck2VSet < 3V 11 = 40mA, Use for Buck2Vset ≥ 3V
Buck2PsvDsc	0	Buck2 Passive Discharge Control 0 = Buck2 passively discharged only in Hard-Reset 1 = Buck2 passively discharged in Hard-Reset or Enable Low

Buck2VSet (0x20)

BIT	7	6	5	4	3	2	1	0
Field	Buck2LowEMI	Buck2RampEn	Buck2VSet[5:0]					
Reset	0b0	0b1						
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck2LowEMI	7	Buck2 Low EMI Mode 0 = Normal operation 1 = Increase rise/fall time on BK2LX by 3x
Buck2RampEn	6	Buck2 Ramp Enable 0 = Voltage setting transition is performed without intermediate steps 1 = Voltage setting transition to a higher value is performed with incremental steps every 20µs
Buck2VSet	5:0	Buck2 Output Voltage Setting 0.7V to (63 x Bk2Step), linear scale, increments of Bk2Step. See Table 3, e.g., for Bk2Step = 25mV: 000000 = 0.7V 000001 = 0.725V … 111111 = 2.275V

Buck2ISet (0x21)

BIT	7	6	5	4	3	2	1	0
Field	Buck2IAdptEn	Buck2SftStrt	Buck2ActDsc	Buck2 FETScale	Buck2ISet[3:0]			
Reset	0b1		0b0					
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION
Buck2IAdptEn	7	Buck2 Adaptive Peak Current Mode 0 = Inductor peak current fixed at the programmed value by means of Buck2ISet 1 = Inductor peak current automatically increased to provide better load regulation
Buck2SftStrt	6	Buck2 Soft-Start Time Buck2 has reduced current capability during soft-start 0 = 50ms 1 = 5ms
Buck2ActDsc	5	Buck2 Active Discharge Control 0 = Buck2 actively discharged only in Hard-Reset 1 = Buck2 actively discharged in Hard-Reset or Enable Low
Buck2FETScale	4	Buck2 Force FET Scaling Reduce the FET size by a factor of two. Used to optimize the efficiency when Buck2ISet must be < 100mA (e.g., to mitigate noise at low frequencies). 0 = FET scaling disabled 1 = FET scaling enabled
Buck2ISet	3:0	Buck2 Inductor Peak Current Setting For the best efficiency, use Buck2ISet = 150mA and 200mA. Linear scale, 25mA increments, settings below 75mA might be limited by the minimum t_{ON} 0000 = 0mA 0001 = 25mA ... 1111 = 375mA

Buck2Ctr (0x22)

BIT	7	6	5	4	3	2	1	0
Field	–	Buck2DVSCfg[2:0]			Buck2MPC3	Buck2MPC2	Buck2MPC1	Buck2MPC0
Reset	–	000			0	0	1	0
Access Type	–	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
Buck2DVSCfg	6:4	Buck2 DVS Configuration 000 = Disabled 001 = DVS Mode 1 Enabled, Buck2 DVS controlled by MPC0 and MPC1 010 = DVS Mode 1 Enabled, Buck2 DVS controlled by MPC0 and MPC2 011 = DVS Mode 1 Enabled, Buck2 DVS controlled by MPC0 and MPC3 100 = DVS Mode 1 Enabled, Buck2 DVS controlled by MPC1 and MPC2 101 = DVS Mode 1 Enabled, Buck2 DVS controlled by MPC1 and MPC3 110 = DVS Mode 1 Enabled, Buck2 DVS controlled by MPC2 and MPC3 111 = DVS Mode 2 Enabled (SPI: MPC0 is $\overline{CS}$, MPC1 is SCLK, MPC2 is DIN.)
Buck2MPC3	3	Buck2 MPC3 Enable Control Only valid when Buck2Seq = 111 and Buck2En = 10. If mutliple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs. 0 = MPC3 does not control Buck2 1 = Buck2 controlled by MPC3
Buck2MPC2	2	Buck2 MPC2 Enable Control Only valid when Buck2Seq = 111 and Buck2En = 10. If mutliple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs. 0 = MPC2 does not control Buck2 1 = Buck2 controlled by MPC2
Buck2MPC1	1	Buck2 MPC1 Enable Control Only valid when Buck2Seq = 111 and Buck2En = 10. If mutliple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs. 0 = MPC1 does not control Buck2 1 = Buck2 controlled by MPC1
Buck2MPC0	0	Buck2 MPC0 Enable Control Only valid when Buck2Seq = 111 and Buck2En = 10. If mutliple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs. 0 = MPC0 does not control Buck2 1 = Buck2 controlled by MPC0

Buck2DVSCfg0 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2DVSVlt0[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck2DVSVlt0	5:0	Buck2 Alternate Output Voltage Setting 1 (Controlling MPCs = 00) 0.7V to (63 x Bk2Step), linear scale, increments of Bk2Step. See Table 3, e.g., for Bk2Step = 25mV: 000000 = 0.7V 000001 = 0.725V … 111111 = 2.275V

Buck2DVSCfg1 (0x24)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2DVSVlt1[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck2DVSVlt1	5:0	Buck2 Alternate Output Voltage Setting 2 (Controlling MPCs = 01) 0.7V to (63 x Bk2Step), linear scale, increments of Bk2Step. See Table 3, e.g., for Bk2Step = 25mV: 000000 = 0.7V 000001 = 0.725V … 111111 = 2.275V

Buck2DVSCfg2 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2DVSVlt2[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck2DVSVlt2	5:0	Buck2 Alternate Output Voltage Setting 3 (Controlling MPCs = 10) 0.7V to (63 x Bk2Step), linear scale, increments of Bk2Step. See Table 3, e.g., for Bk2Step = 25mV: 000000 = 0.7V 000001 = 0.725V … 111111 = 2.275V

Buck2DVSCfg3 (0x26)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2DVSVlt3[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck2DVSVlt3	5:0	Buck2 Alternate Output Voltage Setting 4 (Controlling MPCs = 11) 0.7V to (63 x Bk2Step), linear scale, increments of Bk2Step. See Table 3, e.g., for Bk2Step = 25mV: 000000 = 0.7V 000001 = 0.725V … 111111 = 2.275V

Buck2DVSSPI (0x27)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2SPIVlt[5:0]					
Reset	–	–						
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
Buck2SPIVlt	5:0	Buck2 SPI DVS Readback 0.7V to (63 x Bk2Step), linear scale, increments of Bk2Step. See Table 3, e.g., for Bk2Step = 25mV: 000000 = 0.7V 000001 = 0.725V … 111111 = 2.275V

Buck3Cfg (0x28)

BIT	7	6	5	4	3	2	1	0
Field	Buck3Seq[2:0]			Buck3En[1:0]		Buck3IZCSet[1:0]		Buck3PsvDsc
Reset								0b1
Access Type	Read Only			Write, Read		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION
Buck3Seq	7:5	Buck3 Enable Configuration 000 = Disabled 001 = Reserved 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Reserved 110 = Reserved 111 = Controlled by Buck3En [1:0] after 100% of Boot/POR Process Delay Control
Buck3En	4:3	Buck3 Enable Configuration (effective only when Buck3Seq = 111) 00 = Disabled: BK3OUT not actively discharged unless Hard-Reset/Shut-down/Off mode 01 = Enabled 10 = Controlled by MPC_ (See Buck3MPC_ bits in register 0x2B) 11 = Reserved
Buck3IZCSet	2:1	Buck3 Zero Crossing Current Threshold Optimizes Buck3 for a given voltage setting. 00 = 10mA, Use for Buck3VSet < 1V 01 = 20mA, Use for 1V ≤ Buck3VSet < 1.8V 10 = 30mA, Use for 1.8V ≤ Buck3VSet < 3V 11 = 40mA, Use for Buck3Vset ≥ 3V
Buck3PsvDsc	0	Buck3 Passive Discharge Control 0 = Buck3 passively discharged only in Hard-Reset 1 = Buck3 passively discharged in Hard-Reset or Enable Low

Buck3VSet (0x29)

BIT	7	6	5	4	3	2	1	0
Field	Buck3LowEMI	Buck3RampEn	Buck3VSet[5:0]					
Reset	0b0	0b1						
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck3LowEMI	7	Buck3 Low EMI Mode 0 = Normal operation 1 = Increase rise/fall time on BK3LX by 3x
Buck3RampEn	6	Buck3 Ramp Enable 0 = Voltage setting transition is performed without intermediate steps 1 = Voltage setting transition to a higher value is performed with incremental steps every 20µs
Buck3VSet	5:0	Buck3 Output Voltage Setting 0.7V to (63 x Bk3Step), linear scale, increments of Bk3Step. See Table 3, e.g., for Bk3Step = 50mV: 000000 = 0.7V 000001 = 0.75V … 111111 = 3.85V

Buck1Set[7:0]

BIT	7	6	5	4	3	2	1	0
Field	Buck3IAdptEn	Buck3SftStrt	Buck3ActDsc	Buck3 FETScale	Buck3ISet[3:0]			
Reset	0b1		0b0					
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION
Buck3IAdptEn	7	Buck3 Adaptive Peak Current Mode 0 = Inductor peak current fixed at the programmed value by means of Buck3ISet 1 = Inductor peak current automatically increased to provide better load regulation
Buck3SftStrt	6	Buck3 Soft-Start Time Buck3 has reduced current capability during soft-start 0 = 50ms 1 = 5ms
Buck3ActDsc	5	Buck3 Active Discharge Control 0 = Buck3 actively discharged only in Hard-Reset 1 = Buck3 actively discharged in Hard-Reset or Enable Low
Buck3FETScale	4	Buck3 Force FET Scaling Reduce the FET size by a factor of two. Used to optimize the efficiency when Buck3ISet must be < 100mA (e.g., to mitigate noise at low frequencies). 0 = FET scaling disabled 1 = FET scaling enabled
Buck3ISet	3:0	Buck3 Inductor Peak Current Setting For the best efficiency, use Buck3ISet = 150mA. Linear scale, 25mA increments, settings below 75mA may be limited by the minimum t_{ON} 0000 = 0mA 0001 = 25mA ... 1111 = 375mA

Buck1Set[7:0]

BIT	7	6	5	4	3	2	1	0
Field	–	Buck3DVSCfg[2:0]			Buck3MPC3	Buck3MPC2	Buck3MPC1	Buck3MPC0
Reset	–	000			0	1	0	0
Access Type	–	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
Buck3DVSCfg	6:4	Buck3 DVS Configuration 000 = Disabled 001 = DVS Mode 1 Enabled, Buck3 DVS controlled by MPC0 and MPC1 010 = DVS Mode 1 Enabled, Buck3 DVS controlled by MPC0 and MPC2 011 = DVS Mode 1 Enabled, Buck3 DVS controlled by MPC0 and MPC3 100 = DVS Mode 1 Enabled, Buck3 DVS controlled by MPC1 and MPC2 101 = DVS Mode 1 Enabled, Buck3 DVS controlled by MPC1 and MPC3 110 = DVS Mode 1 Enabled, Buck3 DVS controlled by MPC2 and MPC3 111 = DVS Mode 2 Enabled (SPI: MPC0 is $\overline{CS}$, MPC1 is SCLK, MPC2 is DIN.)
Buck3MPC3	3	Buck3 MPC3 Enable Control Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs. 0 = MPC3 does not control Buck3 1 = Buck3 controlled by MPC3
Buck3MPC2	2	Buck3 MPC2 Enable Control Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs. 0 = MPC2 does not control Buck3 1 = Buck3 controlled by MPC2
Buck3MPC1	1	Buck3 MPC1 Enable Control Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs. 0 = MPC1 does not control Buck3 1 = Buck3 controlled by MPC1
Buck3MPC0	0	Buck3 MPC0 Enable Control Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs. 0 = MPC0 does not control Buck3 1 = Buck3 controlled by MPC0

Buck3DVSCfg0 (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck3DVSVlt0[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck3DVSVlt0	5:0	Buck3 Alternate Output Voltage Setting 1 (Controlling MPCs = 00) 0.7V to (63 x Bk3Step), linear scale, increments of Bk3Step. See Table 3, e.g., for Bk3Step = 50mV: 000000 = 0.7V 000001 = 0.75V … 111111 = 3.85V

Buck3DVSCfg1 (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck3DVSVlt1[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck3DVSVlt1	5:0	Buck3 Alternate Output Voltage Setting 2 (Controlling MPCs = 01) 0.7V to (63 x Bk3Step), linear scale, increments of Bk3Step. See Table 3, e.g., for Bk3Step = 50mV: 000000 = 0.7V 000001 = 0.75V … 111111 = 3.85V

Buck3DVSCfg2 (0x2E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck3DVSVlt2[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck3DVSVlt2	5:0	Buck3 Alternate Output Voltage Setting 3 (Controlling MPCs = 10) 0.7V to (63 x Bk3Step), linear scale, increments of Bk3Step. See Table 3, e.g., for Bk3Step = 50mV: 000000 = 0.7V 000001 = 0.75V … 111111 = 3.85V

Buck3DVSCfg3 (0x2F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck3DVSVlt3[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck3DVSVlt3	5:0	Buck3 Alternate Output Voltage Setting 4 (Controlling MPCs = 11) 0.7V to (63 x Bk3Step), linear scale, increments of Bk3Step. See Table 3, e.g., for Bk3Step = 50mV: 000000 = 0.7V 000001 = 0.75V … 111111 = 3.85V

Buck3DVSSPI (0x30)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck3SPIVlt[5:0]					
Reset	–	–						
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
Buck3SPIVlt	5:0	Buck3 SPI DVS Readback 0.7V to (63 x Bk3Step), linear scale, increments of Bk3Step. See Table 3, e.g., for Bk3Step = 50mV: 000000 = 0.7V 000001 = 0.75V … 111111 = 3.85V

BBstCfg0 (0x31)

BIT	7	6	5	4	3	2	1	0
Field	BBstSeq[2:0]			BBstEn[1:0]		BBstRampEn	BBstMode	BBstPsvDsc
Reset								1
Access Type	Read Only			Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
BBstSeq	7:5	Buck-Boost Enable Configuration 000 = Disabled 001 = Reserved 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Reserved 110 = Reserved 111 = Controlled by BBstEn[1:0] after 100% of Boot/POR Process Delay Control
BBstEn	4:3	Buck-Boost Enable Configuration (effective only when BBstSeq = 111) 00 = Disabled: BBOUT not actively discharged unless Hard-Reset/Shutdown/Off mode 01 = Enabled 10 = Controlled by MPC_ (See BBstMPC_ bits in register 0x34) 11 = Reserved
BBstRampEn	2	Buck-Boost Ramp Enable 0 = Voltage setting transition is performed without intermediate steps 1 = Voltage setting transition to a higher value is performed with incremental steps every 20µs
BBstMode	1	Buck-Boost Operating Mode 0 = Buck-Boost 1 = Buck Only
BBstPsvDsc	0	Buck-Boost Passive Discharge Control 0 = Buck-Boost passively discharged only in Hard-Reset 1 = Buck-Boost passively discharged in Hard-Reset or Enable Low

BBstVSet (0x32)

BIT	7	6	5	4	3	2	1	0
Field	BBstLowEMI	BBstActDsc	BBstVSet[5:0]					
Reset	0	0						
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
BBstLowEMI	7	Buck-Boost Low EMI Mode 0 = Normal operation 1 = Increase rise/fall time on HVLX/LVLX by 3x
BBstActDsc	6	Buck-Boost Active Discharge Control 0 = Buck-Boost actively discharged only in Hard-Reset 1 = Buck-Boost actively discharged in Hard-Reset or Enable Low
BBstVSet	5:0	Buck-Boost Output Voltage Setting 2.5V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V_{BBOUT_UVLO} and are not guaranteed 000000 = 2.5V 000001 = 2.55V … 111100 = 5.5V >111100 = N/A

BBstISet (0x33)

BIT	7	6	5	4	3	2	1	0
Field	BBstIPSet2[3:0]				BBstIPSet1[3:0]			
Reset								
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
BBstIPSet2	7:4	Buck-Boost nominal maximum peak current setting. See Buck-Boost Regulator section for a description of the peak current settings. 0mA to 375mA, linear scale, 25mA increments, settings below 75mA may be limited by the minimum t_{ON}. 0000 = BBstIPSet1 + 0mA 0001 = BBstIPSet1 + 25mA ... 1111 = BBstIPSet1 + 375mA Recommended settings: V_{BBOUT} ≤ 2.65V: 250mA 2.7V < V_{BBOUT} ≤ 3.05V: 225mA 3.1V < V_{BBOUT} ≤ 3.6V: 200mA 3.65V < V_{BBOUT} ≤ 4.35V: 175mA V_{BBOUT} > 4.4V: 150mA
BBstIPSet1	3:0	Buck-Boost nominal peak current setting. Nominal peak current when charging inductor between V_{IN} and GND. See Buck-Boost Regulator section for a description of the peak current settings. 0mA to 375mA, linear scale, 25mA increments, settings below 75mA may be limited by the minimum t_{ON} 0000 = 0mA) 0001 = 25mA ... 1111 = 375mA Recommended settings: V_{BBOUT} ≤ 2.65V: 50mA 2.7V < V_{BBOUT} ≤ 3.05V: 75mA 3.1V < V_{BBOUT} ≤ 3.4V: 100mA 3.45V < V_{BBOUT} ≤ 3.8V: 125mA 3.85V < V_{BBOUT} ≤ 4.15V: 150mA 4.2V < V_{BBOUT} ≤ 4.55V: 175mA 4.6V < V_{BBOUT} ≤ 4.9V: 200mA 4.95V < V_{BBOUT} ≤ 5.3V: 225mA V_{BBOUT} > 5.35V: 250mA

BBstCfg1 (0x34)

BIT	7	6	5	4	3	2	1	0
Field	BBstIPAdptDis	BBstFast	BBZCCmpDis	BBstFETScale	–	–	BBFHighSh[1:0]	
Reset	0				–	–		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
BBstIPAdptDis	7	Adaptive Peak/Valley Current Adjustment Enable 0 = Enabled 1 = Disabled, peak current fixed and is set by BBstIPSet1,2. Valley current is fixed to 0mA
BBstFast	6	Buck-Boost Pre-Trigger Mode Setting 0 = Normal, low quiescent current operation 1 = Increased quiescent mode for fast load transient response. Quiescent current increased to 30µA.
BBZCCmpDis	5	Buck-Boost Zero-Crossing Comparator Disable 0 = Enable 1 = Disable
BBstFETScale	4	Buck-Boost Force FET Scaling Reduce the FET size by factor 2 to optimize the efficiency at light loads 0 = FET scaling disabled 1 = FET scaling enabled
BBFHighSh	1:0	Buck-Boost f_{HIGH} Thresholds Selects the switching frequency threshold f_{HIGH}. If $f_{SW} > f_{HIGH}$ all the blocks are kept ON (I_Q is higher). A small glitch on V_{BBOUT} can be present at the f_{HIGH} crossoverover. 00 = 25khz/6.125Khz 01 = 35Khz/8.25Khz 10 = 50khz/12.5Khz 11 = 100khz/25khz

BBstCtr (0x35)

BIT	7	6	5	4	3	2	1	0
Field	BBstMP-C1FCT	BBstDVSCfg[2:0]			BBstMPC3	BBstMPC2	BBstMPC1	BBstMPC0
Reset					1	0	0	0
Access Type	Write, Read	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
BBstMPC1FCT	7	Buck-Boost FAST mode enable by MPC1. Improves interoperability with MAX86170/171. Tie MPC1 to INT2 on MAX86170/171 if this mode will be used. 0 = FAST status controlled by BBstFast Register 1 = FAST mode controlled by MPC1. MPC1 = 0: FAST disabled MPC1 = 1: FAST enabled, I_Q increased by 30µA
BBstDVSCfg	6:4	Buck-Boost DVS Configuration 000 = Disabled 001 = DVS Mode 1 Enabled, Buck-Boost DVS controlled by MPC0 and MPC1 010 = DVS Mode 1 Enabled, Buck-Boost DVS controlled by MPC0 and MPC2 011 = DVS Mode 1 Enabled, Buck-Boost DVS controlled by MPC0 and MPC3 100 = DVS Mode 1 Enabled, Buck-Boost DVS controlled by MPC1 and MPC2 101 = DVS Mode 1 Enabled, Buck-Boost DVS controlled by MPC1 and MPC3 110 = DVS Mode 1 Enabled, Buck-Boost DVS controlled by MPC2 and MPC3 111 = DVS Mode 2 Enabled (SPI: MPC0 is $\overline{CS}$, MPC1 is SCLK, MPC2 is DIN.)
BBstMPC3	3	Buck-Boost MPC3 Enable Control Only valid when BBstSeq = 111 and BBstEn = 10. If mutliple MPCs are selected, Buck-Boost is controlled by the logical OR of the MPCs. 0 = MPC3 does not control Buck-Boost 1 = Buck-Boost controlled by MPC3
BBstMPC2	2	Buck-Boost MPC2 Enable Control Only valid when BBstSeq = 111 and BBstEn = 10. If mutliple MPCs are selected, Buck-Boost is controlled by the logical OR of the MPCs. 0 = MPC2 does not control Buck-Boost 1 = Buck-Boost controlled by MPC2
BBstMPC1	1	Buck-Boost MPC1 Enable Control Only valid when BBstSeq = 111 and BBstEn = 10. If mutliple MPCs are selected, Buck-Boost is controlled by the logical OR of the MPCs. 0 = MPC1 does not control Buck-Boost 1 = Buck-Boost controlled by MPC1
BBstMPC0	0	Buck-Boost MPC0 Enable Control Only valid when BBstSeq = 111 and BBstEn = 10. If mutliple MPCs are selected, Buck-Boost is controlled by the logical OR of the MPCs. 0 = MPC0 does not control Buck-Boost 1 = Buck-Boost controlled by MPC0

BBstDVSCfg0 (0x36)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BBstDVSVlt0[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BBstDVSVlt0	5:0	Buck-Boost Alternate Output Voltage Setting 1 (Controlling MPCs = 00) 2.5V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V_{BBOUT_UVLO} and are not guaranteed 000000 = 2.5V 000001 = 2.55V … 111100 = 5.5V >111100 = N/A

BBstDVSCfg1 (0x37)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BBstDVSVlt1[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BBstDVSVlt1	5:0	Buck-Boost Alternate Output Voltage Setting 2 (Controlling MPCs = 01) 2.5V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V_{BBOUT_UVLO} and are not guaranteed 000000 = 2.5V 000001 = 2.55V … 111100 = 5.5V >111100 = N/A

BBstDVSCfg2 (0x38)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BBstDVSVlt2[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BBstDVSVlt2	5:0	Buck-Boost Alternate Output Voltage Setting 3 (Controlling MPCs = 10) 2.5V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V_{BBOUT_UVLO} and are not guaranteed 000000 = 2.5V 000001 = 2.55V … 111100 = 5.5V >111100 = N/A

BBstDVSCfg3 (0x39)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BBstDVSVlt3[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BBstDVSVlt3	5:0	Buck-Boost Alternate Output Voltage Setting 4 (Controlling MPCs = 11) 2.6V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V_{BBOUT_UVLO} and are not guaranteed 000000 = 2.5V 000001 = 2.55V … 111100 = 5.5V >111100 = N/A

BBstDVSSPI (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BBstSPIVlt[5:0]					
Reset	–	–						
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
BBstSPIVlt	5:0	Buck-Boost SPI DVS Readback 2.5V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V_{BBOUT_UVLO} and are not guaranteed 000000 = 2.5V 000001 = 2.55V … 111100 = 5.5V >111100 = N/A

LDO1Cfg (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	LDO1Seq[2:0]			LDO1En[1:0]		LDO1ActDsc	LDO1Mode	LDO1PsvDsc
Reset						0		1
Access Type	Read Only			Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
LDO1Seq	7:5	LDO1 Enable Configuration (Read only) 000 = Disabled 001 = Enabled always when BAT/SYS is present 010 = Enabled at 0% of Boot/ POR Process Delay Control 011 = Enabled at 25% of Boot/ POR Process Delay Control 100 = Enabled at 50% of Boot/ POR Process Delay Control 101 = Reserved 110 = Reserved 111 = Controlled by LDO1En [1:0] after 100% of Boot/POR Process Delay Control
LDO1En	4:3	LDO1 Enable Configuration (effective only when LDO1Seq = 111) 00 = Disabled 01 = Enabled 10 = Controlled by MPC_ (See LDO1MPC_ bits in register 0x3D) 11 = Reserved
LDO1ActDsc	2	LDO1 Active Discharge Control 0 = LDO1 output will be actively discharged only in Hard-Reset mode 1 = LDO1 output will be actively discharged in Hard-Reset mode and also when its Enable goes Low
LDO1Mode	1	LDO1 Mode Control When FET is On, the output is unregulated. This setting is internally latched and can change only when the LDO is disabled. 0 = Normal LDO operating mode 1 = Load switch mode. FET is either fully On or Off depending on state of LDO1En.
LDO1PsvDsc	0	LDO1 Passive Discharge Control 0 = LDO1 output will be discharged only entering Off and Hard-Reset modes. 1 = LDO1 output will be discharged only entering Off and Hard-Reset modes and when the enable is Low

LDO1VSet (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	LDO1VSet[4:0]				
Reset	–	–	–					
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
LDO1VSet	4:0	LDO1 Output Voltage Setting Limited by input supply. 0.8V to 3.6V, Linear Scale, 100mV increments 00000 = 0.8V 00001 = 0.9V … 11100 = 3.6V >11101 = N/A

LDO1Ctr (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	LDO1MPC3	LDO1MPC2	LDO1MPC1	LDO1MPC0
Reset	–	–	–	–	0	0	0	1
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
LDO1MPC3	3	LDO1 MPC3 Enable Control Only valid when LDO1Seq = 111 and LDO1En = 10. If mutliple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs. 0 = MPC3 does not control LDO1 1 = LDO1 controlled by MPC3
LDO1MPC2	2	LDO1 MPC2 Enable Control Only valid when LDO1Seq = 111 and LDO1En = 10. If mutliple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs. 0 = MPC2 does not control LDO1 1 = LDO1 controlled by MPC2
LDO1MPC1	1	LDO1 MPC1 Enable Control Only valid when LDO1Seq = 111 and LDO1En = 10. If mutliple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs. 0 = MPC1 does not control LDO1 1 = LDO1 controlled by MPC1
LDO1MPC0	0	LDO1 MPC0 Enable Control Only valid when LDO1Seq = 111 and LDO1En = 10. If mutliple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs. 0 = MPC0 does not control LDO1 1 = LDO1 controlled by MPC0

LDO2Cfg (0x3E)

BIT	7	6	5	4	3	2	1	0
Field	LDO2Seq[2:0]			LDO2En[1:0]		LDO2ActD-sc	LDO2Mode	LDO2Ps-vDsc
Reset						0		1
Access Type	Read Only			Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
LDO2Seq	7:5	LDO2 Enable Configuration (Read only) 000 = Disabled 001 = Reserved 010 = Enabled at 0% of Boot/ POR Process Delay Control 011 = Enabled at 25% of Boot/ POR Process Delay Control 100 = Enabled at 50% of Boot/ POR Process Delay Control 101 = Reserved 110 = Reserved 111 = Controlled by LDO2En [1:0] after 100% of Boot/POR Process Delay Control
LDO2En	4:3	LDO2 Enable Configuration (effective only when LDO2Seq = 111) 00 = Disabled 01 = Enabled 10 = Controlled by MPC_ (See LDO2MPC_ bits in register 0x40) 11 = Reserved
LDO2ActDsc	2	LDO2 Active Discharge Control 0 = LDO2 output will be actively discharged only in Hard-Reset mode 1 = LDO2 output will be actively discharged in Hard-Reset mode and also when its Enable goes Low
LDO2Mode	1	LDO2 Mode Control When FET is On, the output is unregulated. This setting is internally latched and can change only when the LDO is disabled. 0 = Normal LDO operating mode 1 = Load switch mode. FET is either fully On or Off depending on state of LDO2En.
LDO2PsvDsc	0	LDO2 Passive Discharge Control 0 = LDO2 output will be discharged only entering Off and Hard-Reset modes. 1 = LDO2 output will be discharged only entering Off and Hard-Reset modes and when the enable is Low

LDO2VSet (0x3F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	LDO2VSet[4:0]				
Reset	–	–	–					
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
LDO2VSet	4:0	LDO2 Output Voltage Setting Limited by input supply. 0.9V to 4V, Linear Scale, 100mV increments 000000 = 0.9V 000001 = 1V … 11110 = 3.9V 11111 = 4V

LDO2Ctr (0x40)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	LDO2MPC3	LDO2MPC2	LDO2MPC1	LDO2MPC0
Reset	–	–	–	–	0	0	1	0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
LDO2MPC3	3	LDO2 MPC3 Enable Control Only valid when LDO2Seq = 111 and LDO2En = 10. If mutliple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs. 0 = MPC3 does not control LDO2 1 = LDO2 controlled by MPC3
LDO2MPC2	2	LDO2 MPC2 Enable Control Only valid when LDO2Seq = 111 and LDO2En = 10. If mutliple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs. 0 = MPC2 does not control LDO2 1 = LDO2 controlled by MPC2
LDO2MPC1	1	LDO2 MPC1 Enable Control Only valid when LDO2Seq = 111 and LDO2En = 10. If mutliple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs. 0 = MPC1 does not control LDO2 1 = LDO2 controlled by MPC1
LDO2MPC0	0	LDO2 MPC0 Enable Control Only valid when LDO2Seq = 111 and LDO2En = 10. If mutliple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs. 0 = MPC0 does not control LDO2 1 = LDO2 controlled by MPC0

LDO3Cfg (0x41)

BIT	7	6	5	4	3	2	1	0
Field	LDO3Seq[2:0]			LDO3En[1:0]		LDO3ActDsc	LDO3Mode	LDO3PsvDsc
Reset						0		1
Access Type	Read Only			Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
LDO3Seq	7:5	LDO3 Enable Configuration (Read only) 000 = Disabled 001 = Reserved 010 = Enabled at 0% of Boot/ POR Process Delay Control 011 = Enabled at 25% of Boot/ POR Process Delay Control 100 = Enabled at 50% of Boot/ POR Process Delay Control 101 = Reserved 110 = Reserved 111 = Controlled by LDO3En [1:0] after 100% of Boot/POR Process Delay Control
LDO3En	4:3	LDO3 Enable Configuration (effective only when LDO3Seq = 111) 00 = Disabled 01 = Enabled 10 = Controlled by MPC_ (See LDO3MPC_ bits in register 0x43) 11 = Reserved
LDO3ActDsc	2	LDO3 Active Discharge Control 0 = LDO3 output will be actively discharged only in Hard-Reset mode 1 = LDO3 output will be actively discharged in Hard-Reset mode and also when its Enable goes Low
LDO3Mode	1	LDO3 Mode Control When FET is On, the output is unregulated. This setting is internally latched and can change only when the LDO is disabled. 0 = Normal LDO operating mode 1 = Load switch mode. FET is either fully On or Off depending on state of LDO3En.
LDO3PsvDsc	0	LDO3 Passive Discharge Control 0 = LDO3 output will be discharged only entering Off and Hard-Reset modes. 1 = LDO3 output will be discharged only entering Off and Hard-Reset modes and when the enable is Low

LDO3VSet (0x42)

BIT	7	6	5	4	3	2	1	0
Field	–	–	LDO3VSet[5:0]					
Reset	–	–						
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
LDO3VSet	5:0	LDO3 Output Voltage Setting Limited by input supply. 0.5V to 1.95V, Linear Scale, 25mV increments 000000 = 0.5V 000001 = 0.525V … 111010 = 1.95V >111010 = Limited by input supply

LDO3Ctr (0x43)

BIT	7	6	5	4	3	2	1	0
Field	LDO3_ MPC0CNT	LDO3_ MPC0CNF	–	–	LDO3MPC3	LDO3MPC2	LDO3MPC1	LDO3MPC0
Reset	0x0	0x0	–	–	0	1	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
LDO3_MPC0CNT	7	LDO3/MPC0 Control Bit 0 = MPC0 has no effect on the LDO3 1 = LDO3_MPC0CNF is valid and MPC0 function is enabled.
LDO3_MPC0CNF	6	MPC0 configuration bit 0 = MPC0 controls LDO/SW mode of LDO3 (MPC0 = 0 ldo mode, MPC0 = 1 sw mode) 1 = MPC0 controls Enable of LDO3 (MPC0 = 0 disabled, MPC0 = 1 enabled in sw mode)
LDO3MPC3	3	LDO3 MPC3 Enable Control Only valid when LDO3Seq = 111 and LDO3En = 10. If mutliple MPCs are selected, LDO3 is controlled by the logical OR of the MPCs. 0 = MPC3 does not control LDO3 1 = LDO3 controlled by MPC3
LDO3MPC2	2	LDO3 MPC2 Enable Control Only valid when LDO3Seq = 111 and LDO3En = 10. If mutliple MPCs are selected, LDO3 is controlled by the logical OR of the MPCs. 0 = MPC2 does not control LDO3 1 = LDO3 controlled by MPC2
LDO3MPC1	1	LDO3 MPC1 Enable Control Only valid when LDO3Seq = 111 and LDO3En = 10. If mutliple MPCs are selected, LDO3 is controlled by the logical OR of the MPCs. 0 = MPC1 does not control LDO3 1 = LDO3 controlled by MPC1
LDO3MPC0	0	LDO3 MPC0 Enable Control Only valid when LDO3Seq = 111 and LDO3En = 10. If mutliple MPCs are selected, LDO3 is controlled by the logical OR of the MPCs. 0 = MPC0 does not control LDO3 1 = LDO3 controlled by MPC0

LSW1Cfg (0x44)

BIT	7	6	5	4	3	2	1	0
Field	LSW1Seq[2:0]			LSW1En[1:0]		LSW1ActDsc	LSW1LowIq	LSW1PsvDsc
Reset						0		1
Access Type	Read Only			Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
LSW1Seq	7:5	LSW1 Enable Configuration (Read only) 000 = Disabled 001 = Reserved 010 = Enabled at 0% of Boot/ POR Process Delay Control 011 = Enabled at 25% of Boot/ POR Process Delay Control 100 = Enabled at 50% of Boot/ POR Process Delay Control 101 = Reserved 110 = Reserved 111 = Controlled by LSW1En [1:0] after 100% of Boot/POR Process Delay Control
LSW1En	4:3	LSW1 Enable Configuration (effective only when LSW1Seq = 111) 00 = Disabled 01 = Enabled 10 = Controlled by MPC_ (See LSW1MPC_ bits in register 0x45) 11 = Reserved
LSW1ActDsc	2	LSW1 Active Discharge Control 0 = LSW1 output will be actively discharged only in Hard-Reset mode 1 = LSW1 output will be actively discharged in Hard-Reset mode and also when its Enable goes Low
LSW1LowIq	1	LSW1 Low Quiescent Low quiescent mode is achieved by disabling the voltage protection of LSW1. 0 = Voltage Protection Enabled 1 = Voltage Protection Disabled and quiescent is reduced
LSW1PsvDsc	0	LSW1 Passive Discharge Control 0 = LSW1 output will be discharged only entering Off and Hard-Reset modes. 1 = LSW1 output will be discharged only entering Off and Hard-Reset modes and when the enable is Low

LSW1Ctr (0x45)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	LSW1MPC3	LSW1MPC2	LSW1MPC1	LSW1MPC0
Reset	–	–	–	–				
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
LSW1MPC3	3	LSW1 MPC3 Enable Control Only valid when LSW1Seq = 111 and LSW1En = 10. If mutliple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs. 0 = MPC3 does not control LSW1 1 = LSW1 controlled by MPC3
LSW1MPC2	2	LSW1 MPC2 Enable Control Only valid when LSW1Seq = 111 and LSW1En = 10. If mutliple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs. 0 = MPC2 does not control LSW1 1 = LSW1 controlled by MPC2
LSW1MPC1	1	LSW1 MPC1 Enable Control Only valid when LSW1Seq = 111 and LSW1En = 10. If mutliple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs. 0 = MPC1 does not control LSW1 1 = LSW1 controlled by MPC1
LSW1MPC0	0	LSW1 MPC0 Enable Control Only valid when LSW1Seq = 111 and LSW1En = 10. If mutliple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs. 0 = MPC0 does not control LSW1 1 = LSW1 controlled by MPC0

LSW2Cfg (0x46)

BIT	7	6	5	4	3	2	1	0
Field	LSW2Seq[2:0]			LSW2En[1:0]		LSW2ActDsc	LSW2LowIq	LSW2PsvDsc
Reset						0		1
Access Type	Read Only			Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
LSW2Seq	7:5	LSW2 Enable Configuration (Read only) 000 = Disabled 001 = Reserved 010 = Enabled at 0% of Boot/ POR Process Delay Control 011 = Enabled at 25% of Boot/ POR Process Delay Control 100 = Enabled at 50% of Boot/ POR Process Delay Control 101 = Reserved 110 = Reserved 111 = Controlled by LSW2En [1:0] after 100% of Boot/POR Process Delay Control
LSW2En	4:3	LSW2 Enable Configuration (effective only when LSW2Seq = 111) 00 = Disabled 01 = Enabled 10 = Controlled by MPC_ (See LSW2MPC_ bits in register 0x47) 11 = Reserved
LSW2ActDsc	2	LSW2 Active Discharge Control 0 = LSW2 output will be actively discharged only in Hard-Reset mode 1 = LSW2 output will be actively discharged in Hard-Reset mode and also when its Enable goes Low
LSW2LowIq	1	LSW2 Low Quiescent Low quiescent mode is achieved by disabling the voltage protection of LSW2. 0 = Voltage Protection Enabled 1 = Voltage Protection Disabled and quiescent is reduced
LSW2PsvDsc	0	LSW2 Passive Discharge Control 0 = LSW2 output will be discharged only entering Off and Hard-Reset modes. 1 = LSW2 output will be discharged only entering Off and Hard-Reset modes and when the enable is Low

LSW2Ctr (0x47)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	LSW2MPC3	LSW2MPC2	LSW2MPC1	LSW2MPC0
Reset	–	–	–	–				
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
LSW2MPC3	3	LSW2 MPC3 Enable Control Only valid when LSW2Seq = 111 and LSW2En = 10. If mutliple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs. 0 = MPC3 does not control LSW2 1 = LSW2 controlled by MPC3
LSW2MPC2	2	LSW2 MPC2 Enable Control Only valid when LSW2Seq = 111 and LSW2En = 10. If mutliple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs. 0 = MPC2 does not control LSW2 1 = LSW2 controlled by MPC2
LSW2MPC1	1	LSW2 MPC1 Enable Control Only valid when LSW2Seq = 111 and LSW2En = 10. If mutliple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs. 0 = MPC1 does not control LSW2 1 = LSW2 controlled by MPC1
LSW2MPC0	0	LSW2 MPC0 Enable Control Only valid when LSW2Seq = 111 and LSW2En = 10. If mutliple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs. 0 = MPC0 does not control LSW2 1 = LSW2 controlled by MPC0

MPC0Cfg (0x48)

BIT	7	6	5	4	3	2	1	0
Field	MPC0Pin	–	–	MPC0Out	MPC0OD	MPC0HiZB	MPC0Res	MPC0Pup
Reset	0	–	–					
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
MPC0Pin	7	MPC0 State 0 = MPC0 LOW 1 = MPC0 HIGH (if MPC0OD = 0) / Hi-Z (if MPC0OD = 1)
MPC0Out	4	MPC0 Output value Valid only if MPC0 is configured as output (MPC0HiZB = 1) 0 = MPC0 connected to GND 1 = MPC0 open drain off (MPC0OD = 1) / connected to BK3OUT (MPC0OD = 0)
MPC0OD	3	MPC0 Output Configuration Valid only if MPC0 is configured as output (MPC0HiZB = 1) 0 = MPC0 is push-pull connected to BK3OUT 1 = MPC0 is open drain
MPC0HiZB	2	MPC0 Direction 0 = MPC0 is Hi-Z. Input buffer enabled 1 = MPC0 is not Hi-Z. Output buffer enabled
MPC0Res	1	MPC0 Resistor Presence Valid only if MPC0 is configured as input (MPC0HiZB = 0) 0 = Resistor not connected to MPC0 1 = Resistor connected to MPC0
MPC0Pup	0	MPC0 Resistor Configuration Valid only if there is a resistor on MPC0 (MPC0Res = 1) 0 = Pulldown connected to MPC0 1 = Pullup to VCCINT connected MCP0

MPC1Cfg (0x49)

BIT	7	6	5	4	3	2	1	0
Field	MPC1Pin	–	–	MPC1Out	MPC1OD	MPC1HiZB	MPC1Res	MPC1Pup
Reset	0	–	–					
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
MPC1Pin	7	MPC1 State 0 = MPC1 LOW 1 = MPC1 HIGH (if MPC1OD = 0) / Hi-Z (if MPC1OD = 1)
MPC1Out	4	MPC1 Output value Valid only if MPC1 is configured as output (MPC1HiZB = 1) 0 = MPC1 connected to GND 1 = MPC1 open drain off (MPC1OD = 1) / connected to BK3OUT (MPC1OD = 0)
MPC1OD	3	MPC1 Output Configuration Valid only if MPC1 is configured as output (MPC1HiZB = 1) 0 = MPC1 is push-pull connected to BK3OUT 1 = MPC1 is open drain
MPC1HiZB	2	MPC1 Direction 0 = MPC1 is Hi-Z. Input buffer enabled 1 = MPC1 is not Hi-Z. Output buffer enabled
MPC1Res	1	MPC1 Resistor Presence Valid only if MPC1 is configured as input (MPC1HiZB = 0) 0 = Resistor not connected to MPC1 1 = Resistor connected to MPC1
MPC1Pup	0	MPC1 Resistor Configuration Valid only if there is a resistor on MPC1 (MPC1Res = 1) 0 = Pulldown connected to MPC1 1 = Pullup to VCCINT connected MCP1

MPC2Cfg (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	MPC2Pin	–	–	MPC2Out	MPC2OD	MPC2HiZB	MPC2Res	MPC2Pup
Reset	0	–	–					
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
MPC2Pin	7	MPC2 State 0 = MPC2 LOW 1 = MPC2 HIGH (if MPC2OD = 0) / Hi-Z (if MPC2OD = 1)
MPC2Out	4	MPC2 Output value Valid only if MPC2 is configured as output (MPC2HiZB = 1) 0 = MPC2 connected to GND 1 = MPC2 open drain off (MPC2OD = 1) / connected to BK3OUT (MPC2OD = 0)
MPC2OD	3	MPC2 Output Configuration Valid only if MPC2 is configured as output (MPC2HiZB = 1) 0 = MPC2 is push-pull connected to BK3OUT 1 = MPC2 is open drain
MPC2HiZB	2	MPC2 Direction 0 = MPC2 is Hi-Z. Input buffer enabled 1 = MPC2 is not Hi-Z. Output buffer enabled
MPC2Res	1	MPC2 Resistor Presence Valid only if MPC2 is configured as input (MPC2HiZB = 0) 0 = Resistor not connected to MPC2 1 = Resistor connected to MPC2
MPC2Pup	0	MPC2 Resistor Configuration Valid only if there is a resistor on MPC2 (MPC2Res = 1) 0 = Pulldown connected to MPC2 1 = Pullup to VCCINT connected MCP2

MPC3Cfg (0x4B)

BIT	7	6	5	4	3	2	1	0
Field	MPC3Pin	–	–	MPC3Out	MPC3OD	MPC3HiZB	MPC3Res	MPC3Pup
Reset	0	–	–					
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
MPC3Pin	7	MPC3 State 0 = MPC3 LOW 1 = MPC3 HIGH (if MPC3OD = 0) / Hi-Z (if MPC3OD = 1)
MPC3Out	4	MPC3 Output value Valid only if MPC3 is configured as output (MPC3HiZB = 1) 0 = MPC3 connected to GND 1 = MPC3 open drain off (MPC3OD = 1) / connected to BK3OUT (MPC3OD = 0)
MPC3OD	3	MPC3 Output Configuration Valid only if MPC3 is configured as output (MPC3HiZB = 1) 0 = MPC3 is push-pull connected to BK3OUT 1 = MPC3 is open drain
MPC3HiZB	2	MPC Direction 0 = MPC3 is Hi-Z. Input buffer enabled 1 = MPC3 is not Hi-Z. Output buffer enabled
MPC3Res	1	MPC3 Resistor Presence Valid only if MPC3 is configured as input (MPC3HiZB = 0) 0 = Resistor not connected to MPC3 1 = Resistor connected to MPC3
MPC3Pup	0	MPC3 Resistor Configuration Valid only if there is a resistor on MPC3 (MPC3Res = 1) 0 = Pulldown connected to MPC3 1 = Pullup to VCCINT connected MCP3

PFN (0x4C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	PFN2Pin	PFN1Pin
Reset	–	–	–	–	–	–		
Access Type	–	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
PFN2Pin	1	Status of PFN2 0 = PFN2 not active 1 = PFN2 active
PFN1Pin	0	Status of PFN1 0 = PFN1 not active 1 = PFN1 active

BootCfg (0x4D)

BIT	7	6	5	4	3	2	1	0
Field	PwrRstCfg[3:0]				SftRstCfg	BootDly[1:0]		ChgAlwTry
Reset								
Access Type	Read Only				Read Only	Read Only		Read Only

BITFIELD	BITS	DESCRIPTION
PwrRstCfg	7:4	Power Reset Configuration Determines how the device turns on, off, and enters hard/soft reset. See Table 1 for PwrRstCfg values and their associated behaviors.
SftRstCfg	3	Soft-Reset Configuration Indicates whether registers are held or reset to default during a soft-reset. 0 = Hold register contents 1 = Reset registers to default
BootDly	2:1	Boot Delay The boot period when the sequencing engine turns on features with sequence bits 010, 011, and 100. 00 = 80ms 01 = 120ms 10 = 220ms 11 = 420ms
ChgAlwTry	0	UVLO Automatic Retry If a SYS UVLO condition occurs during the boot process 0 = Part latches off until CHGIN is removed and replaced 1 = Part retries to boot after delay

PwrCfg (0x4E)

BIT	7	6	5	4	3	2	1	0
Field	ThmtoMonEn	ThmtoMonAbr	–	–	–	–	–	StayOn
Reset			–	–	–	–	–	
Access Type	Write, Read	Write, Read	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
ThmtoMonEn	7	One-Shot THM Monitor Enable Writing 1 triggers a one-shot measurement sequence to measure THM on IV-MON using the TPUEXT reference (see THM One-Shot Measurement section in Detailed Description). This bit must be manually cleared before triggering a new measurement.
ThmtoMonAbr	6	One-Shot THM Monitor Abort Writing 1 aborts a one-shot THM measurement sequence. This bit must be manually cleared.
StayOn	0	StayOn This bit is used to ensure that the processor booted correctly. This bit must be set within 5s of power-on to prevent the part from shutting down and returning to the power-off condition. This bit has no effect after being set. 0 = Shut down 5s after power-on 1 = Stay on

PwrCmd (0x4F)

BIT	7	6	5	4	3	2	1	0
Field	PowerCommand[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PowerCommand	7:0	Power Command Register Writing the following values issues the command listed: 0xB2 = places the part in off mode 0xC3 = issues a hard-reset (power cycle) 0xD4 = issues a soft-reset (reset pulse only) After the written value has been validated by the internal logic, this register is cleared automatically. Any other commands are ignored. See Table 1 for the available PwrCmd for each PwrRstCfg value.

LockMsk (0x52)

BIT	7	6	5	4	3	2	1	0
Field	LDO3Lck	LDO2Lck	LDO1Lck	BBstLck	Bk3Lck	Bk2Lck	Bk1Lck	ChgLck
Reset								
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
LDO3Lck	7	Lock Mask for LDO3 Registers 0 = LDO3 Registers not masked from locking/unlocking 1 = LDO3 Registers masked from locking/unlocking
LDO2Lck	6	Lock Mask for LDO2 Registers 0 = LDO2 Registers not masked from locking/unlocking 1 = LDO2 Registers masked from locking/unlocking
LDO1Lck	5	Lock Mask for LDO1 Registers 0 = LDO1 Registers not masked from locking/unlocking 1 = LDO1 Registers masked from locking/unlocking
BBstLck	4	Lock Mask for Buck-Boost Registers 0 = Buck-Boost Registers not masked from locking/unlocking 1 = Buck-Boost Registers masked from locking/unlocking
Bk3Lck	3	Lock Mask for Buck3 Registers 0 = Buck3 Registers not masked from locking/unlocking 1 = Buck3 Registers masked from locking/unlocking
Bk2Lck	2	Lock Mask for Buck2 Registers 0 = Buck2 Registers not masked from locking/unlocking 1 = Buck2 Registers masked from locking/unlocking
Bk1Lck	1	Lock Mask for Buck1 Registers 0 = Buck1 Registers not masked from locking/unlocking 1 = Buck1 Registers masked from locking/unlocking
ChgLck	0	Lock Mask for Charger Registers 0 = Charger Registers not masked from locking/unlocking 1 = Charger Registers masked from locking/unlocking

LockUnlock (0x53)

BIT	7	6	5	4	3	2	1	0
Field	PASSWORD[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PASSWORD	7:0	Lock/Unlock Password Locks or unlocks all unmasked functions set in the Lock Mask register 0x52 when the correct password is written. Reading this register returns the current lock state of the functions. Locked functions return 1 and unlocked functions return 0. Functions are organized in the same order as register 0x52. 0x55 = Unlock unmasked functions 0xAA = Lock unmasked functions All other codes = No effect

Applications Information

I²C Interface

The MAX20345 contains an I²C-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

Start, Stop, and Repeated Start Conditions

When writing to the MAX20345 using I²C, the master sends a START condition (S) followed by the MAX20345 I²C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I²C slave. See Figure 15.

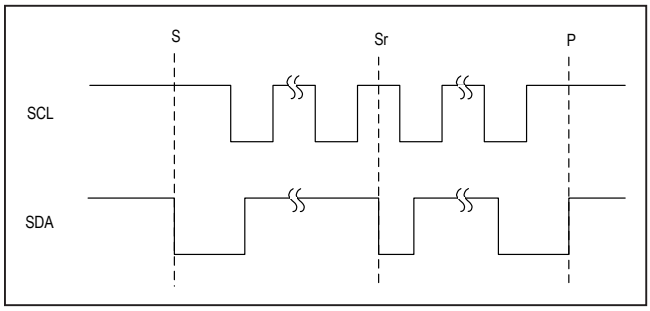


Figure 15. I²C START, STOP, and REPEATED START Conditions

Slave Address

Set the Read/$\overline{\text{Write}}$ bit high to configure the MAX20345 to read mode. Set the Read/$\overline{\text{Write}}$ bit low to configure the MAX20345 to write mode. The address is the first byte of information sent to the MAX20345 after the START condition.

Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *Start, Stop, and Repeated Start Conditions* section). Both SDA and SCL remain high when the bus is not active.

Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device (Figure 16). The following procedure describes the single byte write operation:

- The master sends a START condition
- The master sends the 7-bit slave address plus a write bit (low)
- The addressed slave asserts an ACK on the data line
- The master sends the 8-bit register address
- The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- The master sends 8 data bits
- The slave asserts an ACK on the data line
- The master generates a STOP condition

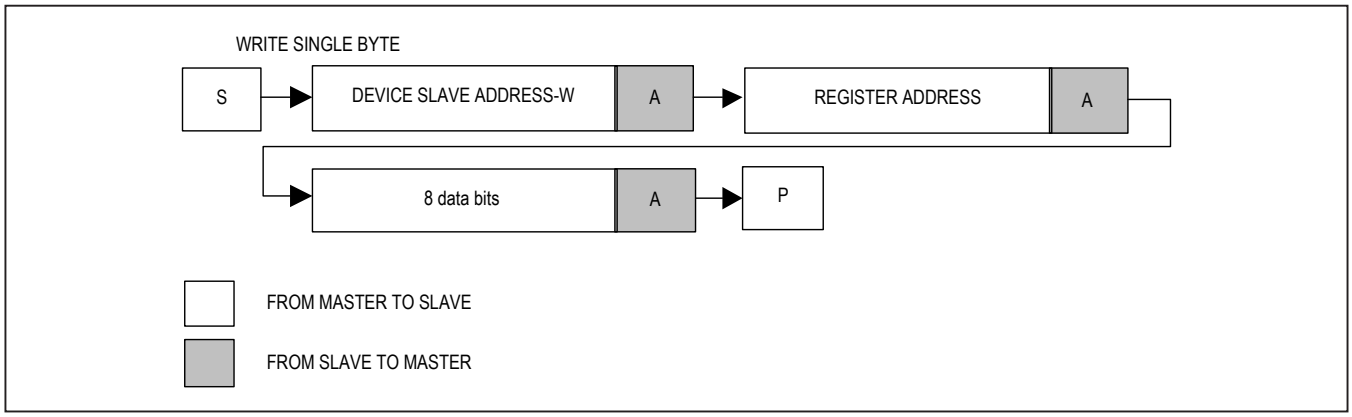


Figure 16. Write Byte Sequence

Burst Write

In this operation, the master sends an address and multiple data bytes to the slave device (Figure 17). The slave device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

- The master sends a START condition
- The master sends the 7-bit slave address plus a write bit (low)
- The addressed slave asserts an ACK on the data line
- The master sends the 8-bit register address
- The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- The master sends 8 data bits
- The slave asserts an ACK on the data line
- Repeat 6 and 7 N-1 times
- The master generates a STOP condition

Single Byte Read

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (Figure 18). The following procedure describes the single byte read operation:

- The master sends a START condition
- The master sends the 7-bit slave address plus a write bit (low)
- The addressed slave asserts an ACK on the data line
- The master sends the 8-bit register address
- The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- The master sends a REPEATED START condition
- The master sends the 7-bit slave address plus a read bit (high)
- The addressed slave asserts an ACK on the data line
- The slave sends 8 data bits
- The master asserts a NACK on the data line
- The master generates a STOP condition

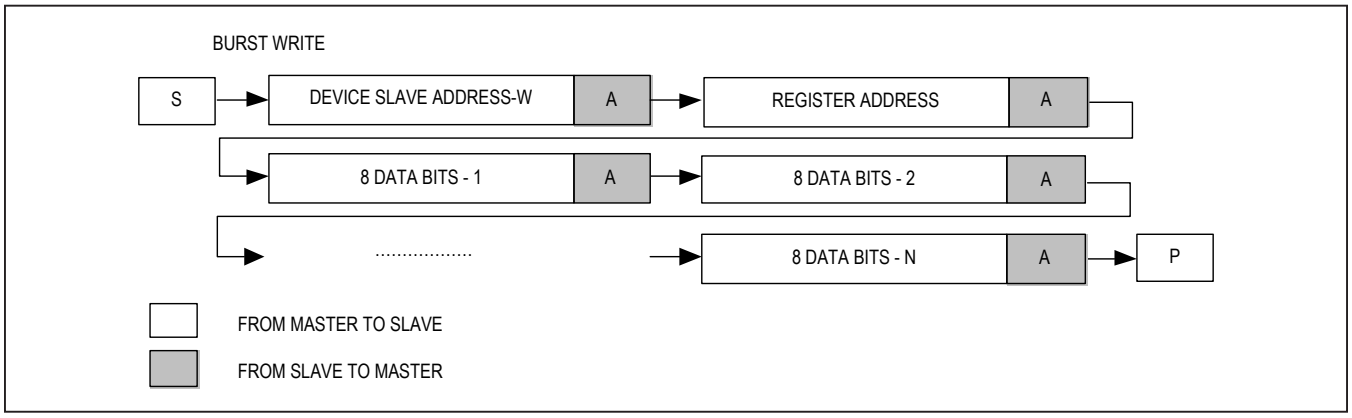


Figure 17. Burst Write Sequence

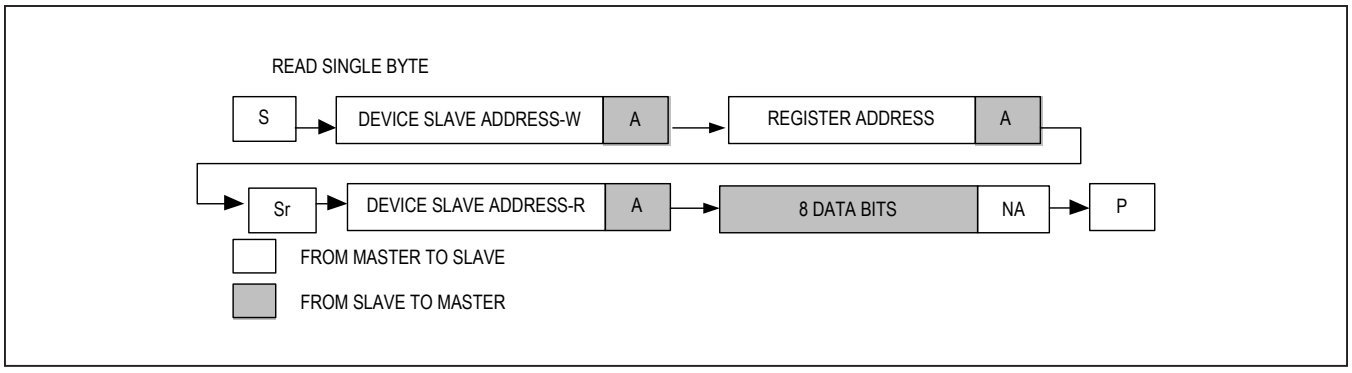


Figure 18. Read Byte Sequence

Burst Read

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (Figure 19). The following procedure describes the burst byte read operation:

- The master sends a START condition
- The master sends the 7-bit slave address plus a write bit (low)
- The addressed slave asserts an ACK on the data line
- The master sends the 8-bit register address
- The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- The master sends a REPEATED START condition
- The master sends the 7-bit slave address plus a read bit (high)
- The slave asserts an ACK on the data line
- The slave sends 8 data bits
- The master asserts an ACK on the data line
- Repeat 9 and 10 N-2 times
- The slave sends the last 8 data bits
- The master asserts a NACK on the data line
- The master generates a STOP condition

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX20345 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (see Figure 20). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

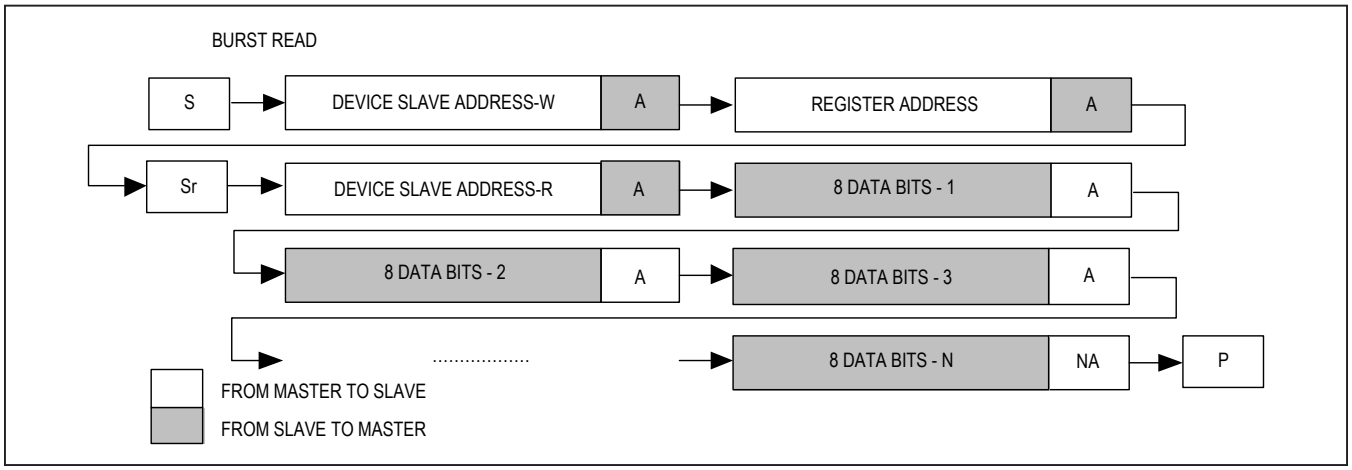


Figure 19. Burst Read Sequence

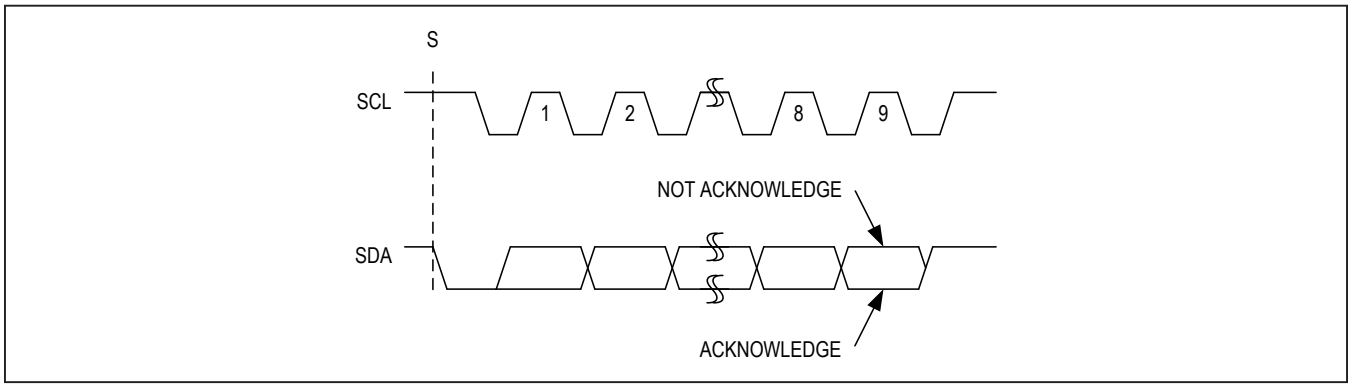


Figure 20. Acknowledge Bits

Default Bits

Table 3. Register Bit Default Values

REGISTER BITS	MAX20345A	MAX20345B	MAX20345I	MAX20345J	MAX20345K	MAX20345L	MAX20345M
SysMinVlt	4.0V	4.0V	4.0V	4.0V	4.0V	3.6V	4V
ILimBlank	Disabled, minimum response time	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
ILimCntl	450mA	450mA	1000mA	450mA	450mA	90mA	90mA
IChgDone	30% IFCHG	5% IFCHG	5% IFCHG	10% IFCHG	5% IFCHG	5% IFCHG	10% IFCHG
BatReChg	BatReg - 70mV	BatReg - 70mV	BatReg - 70mV	BatReg - 120mV	BatReg - 70mV	BatReg - 70mV	BatReg - 120mV
BatReg	4.20V	4.20V	4.35V	4.20V	4.40V	4.40V	4.40V
ChgEn	Enabled	Enabled	Enabled	Enabled	Disabled	Enabled	Enabled
PChgTmr	240min	240min	240min	240min	30min	30min	30min
VPChg	3.00V	3.00V	3.15V	3.15V	3.15V	3.00V	2.55V
IPChg	5% IFCHG	5% IFCHG	20% IFCHG	20% IFCHG	5% IFCHG	10% IFCHG	5% IFCHG
ChgStepRise	4.00V	4.00V	4.10V	4.10V	4.00V	4.20V	4.30V
ChgAutoStp	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
ChgAutoReSta	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
MtChgTmr	60min	60min	15min	30min	60min	15min	0min
FChgTmr	300min	300min	300min	300min	150min	300min	150min
ChgIStep	30% IFCHG	30% IFCHG	80% IFCHG	100% IFCHG	100% IFCHG	50% IFCHG	100% IFCHG
ChgStepHyst	400mV	400mV	400mV	400mV	400mV	400mV	400mV
Buck1VSet	1.200V	1.10V	1.00V	1.20V	0.72V	1.10V	0.70V
Buck1En	Disabled	MPC Reg Defined	Enabled	Disabled	Disabled	Enabled	Disabled
Buck1IZCSet	20mA	20mA	10mA	10mA	10mA	20mA	10mA
ThmEn	Disabled	Disabled	Disabled	Charge in T1-T3	Charge in T1-T3	Charge in T1-T3	Charge in T1-T4
Buck1ISet	150mA	150mA	200mA	150mA	150mA	150mA	150mA
Buck2VSet	1.800V	1.800V	1.800V	1.800V	1.850V	1.800V	1.800V
Buck2En	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
Buck2IZCSet	20mA	30mA	30mA	30mA	30mA	30mA	30mA
Buck1SftStrt	50ms Soft-Start	50ms Soft-Start	100ms Soft-Start	100ms Soft-Start	100ms Soft-Start	50ms Soft-Start	100ms Soft-Start
Buck1FETScale	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Buck2ISet	150mA	150mA	200mA	150mA	150mA	150mA	150mA
Buck3VSet	3.100V	3.10V	1.80V	3.30V	3.20V	3.10V	1.80V
Buck3En	Enabled	Enabled	Disabled	Disabled	Disabled	Enabled	Disabled
Buck3IZCSet	40mA	40mA	30mA	30mA	40mA	40mA	30mA
Buck2SftStrt	50ms SoftStart	50ms Soft-Start	100ms Soft-Start	100ms Soft-Start	100ms Soft-Start	50ms Soft-Start	100ms Soft-Start
Buck2FETScale	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled

Table 3. Register Bit Default Values (continued)

REGISTER BITS	MAX20345A	MAX20345B	MAX20345I	MAX20345J	MAX20345K	MAX20345L	MAX20345M
Buck3ISet	150mA	150mA	200mA	150mA	150mA	150mA	150mA
BBstVSet	3.30V	3.50V	5.00V	5.00V	5.00V	3.10V	5.00V
BBstEn	Enabled	Disabled	Disabled	Enabled	Disabled	Disabled	Disabled
BBstMode	Buck-Boost	Buck-Boost	Buck-Boost	Buck-Boost	Buck-Boost	Buck Only	Buck-Boost
Buck3SftStrt	50ms Soft-Start	100ms Soft-Start	100ms Soft-Start	100ms Soft-Start	100ms Soft-Start	50ms Soft-Start	100ms Soft-Start
Buck3FETScale	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
BBstIPSet2	BBstIPSet1 + 200mA	IPSet1 + 200mA	IPSet1 + 150mA	IPSet1 + 150mA	IPSet1 + 150mA	IPSet1 + 100mA	IPSet1 + 150mA
BBstIPSet1	100mA	125mA	275mA	225mA	225mA	150mA	225mA
LDO1Mode	Load Switch	LDO	LDO	LDO	LDO	LDO	LDO
BBstFETScale	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
LDO2Mode	LDO	LDO	LDO	LDO	LDO	LDO	LDO
LDO1VSet	1.8V	1.8V	1.8V	1.8V	3.2V	1.8V	1.8V
LDO1En	Enabled	Enabled	Disabled	Disabled	Disabled	Enabled	Disabled
LDO3Mode	LDO	LDO	LDO	LDO	Load Switch	LDO	LDO
LDO2VSet	3.1V	3.1V	1.8V	4.0V	3.2V	1.8V	1.8V
LDO2En	Disabled	Disabled	Disabled	Disabled	Disabled	Enabled	Disabled
LDO3VSet	1.2V	1.8V	1.8V	1.95V	0.70V	1.2V	0.7V
LDO3En	Disabled	Enabled	Disabled	Disabled	Disabled	Disabled	Disabled
BootDly	80ms	80ms	120ms	120ms	420ms	220ms	120ms
ChgAlwTry	Retry	Retry	Retry	Retry	Retry	Retry	Retry
LSW2En	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
LSW2LowIq	No voltage protection	No voltage protection	Voltage protection	Voltage Protection	No Voltage Protection	Voltage Protection	No Voltage Protection
LSW1En	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Enabled
LSW1LowIq	No voltage protection	No voltage protection	Voltage protection	Voltage Protection	No Voltage Protection	Voltage Protection	No Voltage Protection
UsbOkselect	CHGIN Rise	CHGIN Rise	CHGIN Rise	CHGIN Rise	CHGIN Rise	CHGIN Rise	CHGIN Rise
PwrRstCfg	0b0110	0b0110	0b0111	0b0110	0b1000	0b0111	0b0010
SftRstCfg	Reset Registers	Reset Regs	Reset Regs	Reset Regs	Reset Regs	Reset Regs	Reset Regs
IBatOc	1600mA	1600mA	1600mA	1600mA	1000mA	1600mA	200mA
FrshBatDis	1	Charge	Charge	Charge	Charge	Charge	Charge
Bk2Step	25mV	25mV	25mV	25mV	25mV	25mV	25mV
Buck1Seq	Buck1En After 100%	Buck1En After 100%	50%	Buck1En After 100%	Buck1En After 100%	50%	Buck1En After 100%
Bk1Step	10mV	10mV	10mV	10mV	10mV	10mV	10mV
Bk3Step	50mV	50mV	50mV	50mV	50mV	50mV	50mV

Table 3. Register Bit Default Values (continued)

REGISTER BITS	MAX20345A	MAX20345B	MAX20345I	MAX20345J	MAX20345K	MAX20345L	MAX20345M
Buck2Seq	Buck2En After 100%	Buck2En After 100%	0%	Buck2En After 100%	25%	25%	Buck2En After 100%
LDO1Seq	LDO1En After 100%	Always On	LDO1En After 100%	LDO1En After 100%	LDO1En After 100%	Always On	LDO1En After 100%
BBstSeq	0%	BBstEn After 100%	BBstEn After 100%	BBstEn After 100%	BBstEn After 100%	BBstEn After 100%	BBstEn After 100%
Buck3Seq	Buck3En After 100%	Buck3En After 100%	Buck3En After 100%	Buck3En After 100%	Buck3En After 100%	25%	Buck3En After 100%
LSW1Seq	LSW1En After 100%	LSW1En After 100%	LSW1En After 100%	LSW1En After 100%	LSW1En After 100%	LSW1En After 100%	LSW1En After 100%
LDO3Seq	LDO3En After 100%	LDO3En After 100%	LDO3En After 100%	LDO3En After 100%	Disabled	LDO3En After 100%	LDO3En After 100%
LDO2Seq	LDO2En After 100%	LDO2En After 100%	LDO2En After 100%	LDO2En After 100%	LDO2En After 100%	25%	LDO2En After 100%
PFN1RInt	Resistor connected	Resistor Connected	Resistor Connected	Resistor Connected	Resistor Connected	Connect Resistor	Connect Resistor
PFN2RInt	No Resistor	No Resistor	No Resistor	Resistor Connected	Resistor Connected	No Resistor	Connect Resistor
GlbPsvDsc	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
LSW2Seq	LSW2En After 100%	LSW2En After 100%	LSW2En After 100%	LSW2En After 100%	LSW2En After 100%	LSW2En After 100%	LSW2En After 100%
BBstIAdptDis	Adaptive IPEAK	Adaptive IPEAK	Adaptive IPEAK	Adaptive IPEAK	Adaptive IPEAK	Adaptive IPEAK	Fixed IPEAK
PFN1PUD	Pullup	Pullup	Pullup	Pullup	Pullup	Pull-Up	Pull-down
PFN2PUD	N/A	N/A	N/A	Pullup	Pullup	N/A	Pull-down
JEITASet	T4 = 25.53%, T3 = 32.94%	T4 = 25.53%, T3 = 32.94%	T4 = 25.53%, T3 = 32.94%	T4 = 25.53%, T3 = 32.94%	T4 = 25.53%, T3 = 32.94%	T4 = 25.53%, T3 = 32.94%	T4 = 32.94%, T3 = 50.20%
ILimMax	1000mA	1000mA	1000mA	1000mA	1000mA	1000mA	450mA
TShdn	120°C	120°C	120°C	120°C	120°C	120°C	120°C

Register Defaults

Table 4. Register Default Values

REGISTER	NAME	MAX20345A
0x00	ChipID	0x07
0x01	ChipRev	0x01
0x09	IntMask0	0x00
0x0A	IntMask1	0x00
0x0B	IntMask2	0x00
0x0C	ILimCntl	0x86
0x0D	ChgCntl0	0x07

REGISTER	NAME	MAX20345A
0x0E	ChgCntl1	0x63
0x0F	ChgTmr	0xFB
0x10	StepChgCfg0	0x34
0x11	StepChgCfg1	0x01
0x12	ThmCfg0	0x1F
0x13	ThmCfg1	0x1F
0x14	ThmCfg2	0x1F

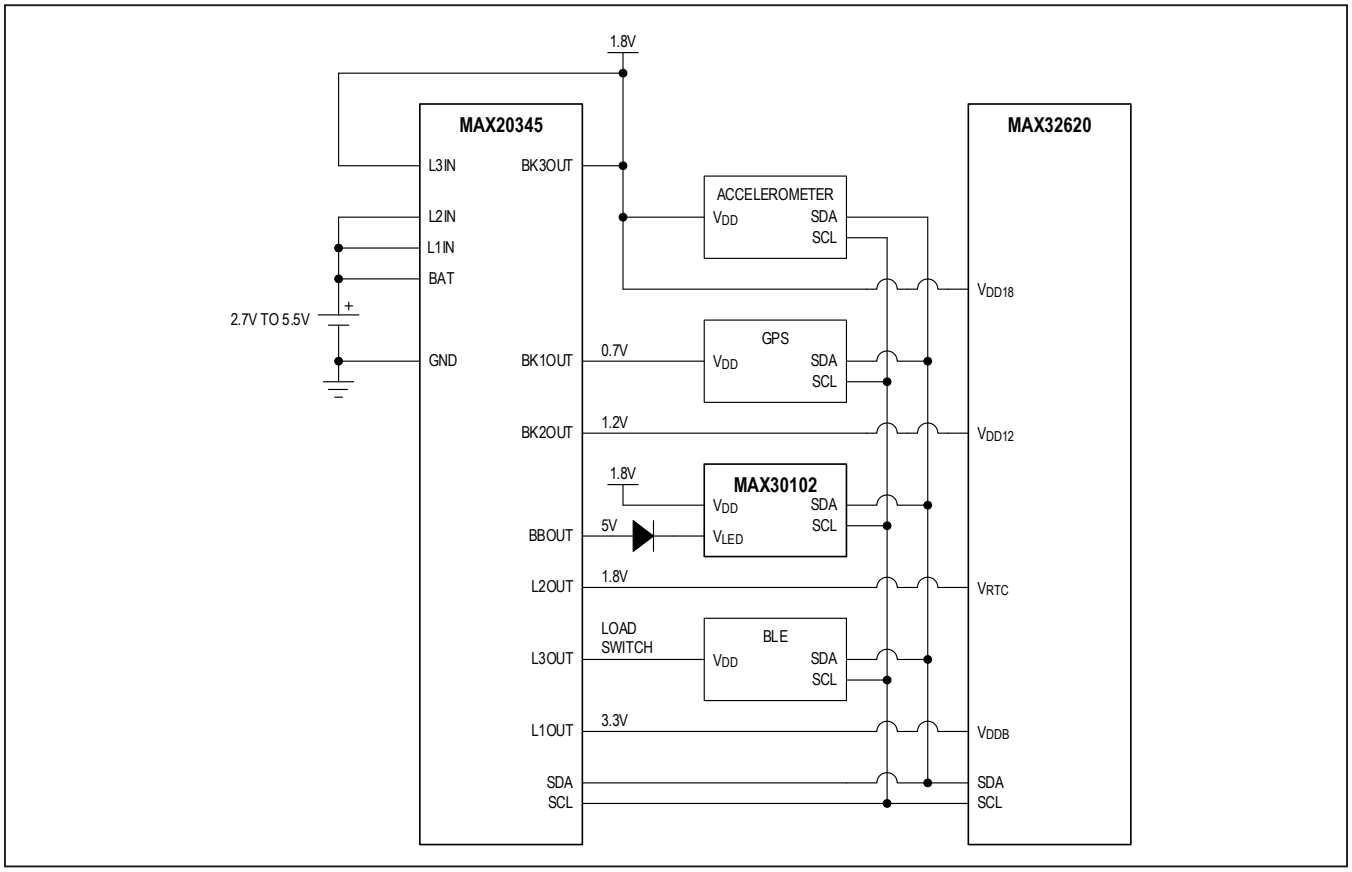
Table 4. Register Default Values (continued)

REGISTER	NAME	MAX20345A
0x15	MONCfg	0x10
0x16	Buck1Cfg	0xE3
0x17	Buck1VSet	0x70
0x18	Buck1ISet	0xC6
0x19	Buck1Ctr	0x01
0x1A	Buck1DVSCfg0	0x00
0x1B	Buck1DVSCfg1	0x00
0x1C	Buck1DVSCfg2	0x00
0x1D	Buck1DVSCfg3	0x00
0x1E	Buck1DVSSPI	0x00
0x1F	Buck2Cfg	0xED
0x20	Buck2VSet	0x6C
0x21	Buck2ISet	0xC6
0x22	Buck2Ctr	0x02
0x23	Buck2DVSCfg0	0x00
0x24	Buck2DVSCfg1	0x00
0x25	Buck2DVSCfg2	0x00
0x26	Buck2DVSCfg3	0x00
0x27	Buck2DVSSPI	0x00
0x28	Buck3Cfg	0xEF
0x29	Buck3VSet	0x70
0x2A	Buck3ISet	0xC6
0x2B	Buck3Ctr	0x04
0x2C	Buck3DVSCfg0	0x00
0x2D	Buck3DVSCfg1	0x00
0x2E	Buck3DVSCfg2	0x00
0x2F	Buck3DVSCfg3	0x00
0x30	Buck3DVSSPI	0x00
0x31	BBstCfg0	0x4D
0x32	BBstVSet	0x10

REGISTER	NAME	MAX20345A
0x33	BBstISet	0x84
0x34	BBstCfg1	0x23
0x35	BBstCtr	0x08
0x36	BBstDVSCfg0	0x00
0x37	BBstDVSCfg1	0x00
0x38	BBstDVSCfg2	0x00
0x39	BBstDVSCfg3	0x00
0x3A	BBstDVSSPI	0x00
0x3B	LDO1Cfg	0xEC
0x3C	LDO1VSet	0x0A
0x3D	LDO1Ctr	0x01
0x3E	LDO2Cfg	0xE1
0x3F	LDO2VSet	0x16
0x40	LDO2Ctr	0x02
0x41	LDO3Cfg	0xE1
0x42	LDO3VSet	0x1C
0x43	LDO3Ctr	0x04
0x44	LSW1Cfg	0xE3
0x45	LSW1Ctr	0x00
0x46	LSW2Cfg	0xE3
0x47	LSW2Ctr	0x00
0x48	MPC0Cfg	0x00
0x49	MPC1Cfg	0x00
0x4A	MPC2Cfg	0x00
0x4B	MPC3Cfg	0x00
0x4D	BootCfg	0x6A
0x4E	PwrCfg	0x01
0x52	LockMsk	0x00
0x53	LockUnlock	0xFF

Typical Application Circuits

Sports Watch with Heart Rate Monitoring



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX20345AEWN+	-40°C to +85°C	56-WLP
MAX20345AEWN+T	-40°C to +85°C	56-WLP
MAX20345BEWN+	-40°C to +85°C	56-WLP
MAX20345BEWN+T	-40°C to +85°C	56-WLP
MAX20345IEWN+	-40°C to +85°C	56-WLP
MAX20345IEWN+T	-40°C to +85°C	56-WLP
MAX20345JEWN+	-40°C to +85°C	56-WLP
MAX20345JEWN+T	-40°C to +85°C	56-WLP
MAX20345KEWN+	-40°C to +85°C	56-WLP
MAX20345KEWN+T	-40°C to +85°C	56-WLP
MAX20345LEWN+	-40°C to +85°C	56-WLP
MAX20345LEWN+T	-40°C to +85°C	56-WLP
MAX20345MEWN+	-40°C to +85°C	56-WLP
MAX20345MEWN+T	-40°C to +85°C	56-WLP

+ Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/18	Initial release	—
1	11/18	Updated the title, *General Description* section; replaced all *Typical Operating Characteristics* and corrected bit names; corrected typos	1–126
2	12/18	Added new TOC06–TOC09 and renumbered subsequent and renumbered remaining TOCs; corrected some typos in TOCs and added the *I²C Interface Overview* section	27–33, 57
3	2/20	Updated the *Electrical Characteristics*, *Pin Description,* and *Buck-Boost Regulator* sections; updated the *Register Map*, *Register 0x18*, and bit 3 information for Registers 0x04, 0x07, and 0x0A; corrected Reset information for Registers 0x00 and 0x01, and Description for Bit 6 for Registers 0x18, 0x21, and 0x2A; added new Figure 5 and renumbered subsequent figures; corrected typo	9, 20–22, 35, 51, 58, 61, 63, 65, 67, 79, 85, 91
4	12/20	Updated Table 3; added MAX20345BEWN+ and MAX20345BEWN+T as future parts, and MAX20345IEWN+ and MAX20345IEWN+T to the *Ordering Information* table	122–123, 125
5	2/21	Updated Figures 1a–1g and Table 3; added MAX20345JEWN+ and MAX20345JEWN+T, MAX20345KEWN+ and MAX20345KEWN+T to the *Ordering Information* table; corrected the part number for MAX20345IEWN+ and MAX20345IEWN+T in the *Ordering Information* table	37–45, 122, 125
6	3/21	Removed future product designation from MAX20345JEWN+ and MAX20345JEWN+T	126
7	5/21	Removed future product designation from MAX20345KEWN+ and MAX20345KEWN+T, updated Typical Application Circuit	126
8	8/21	Added caption for registers ILimCntl, ChrCntl0, ChgCntl1, ChgTmr, StepChgChg0, StepChgCfg1, ThmCfg0, ThmCfg1, ThmCfg2	58, 69–75
9	9/21	Removed future product designation from MAX20345BEWN+ and MAX20345BEWN+	126
10	5/22	Updated Table 3; added MAX20345LEWN+ and MAX20345LEWN+T to the *Ordering Information* table	122–124, 126
11	9/23	Updated Table 3; added MAX20345MEWN+ and MAX20345MEWN+T to the *Ordering Information* table.	122–124, 126