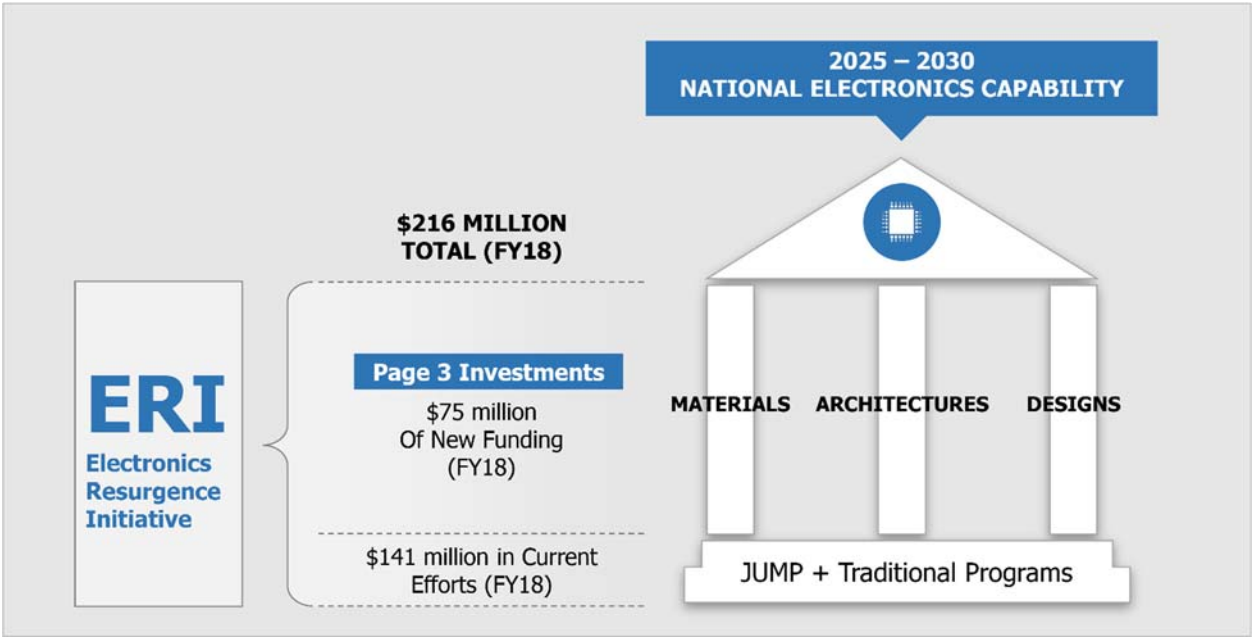
Microsystems Technology Office
Broad Agency Announcement
Electronics Resurgence Initiative: Page 3 Investments
Design Thrust
HR001117S0054
September 13, 2017

Foreword

In his seminal 1965 paper, Gordon Moore, one of the pioneers of the ongoing microelectronics revolution, famously predicted a trajectory of progress in which the transistor count of integrated circuits would double every two years while the cost per transistor would decrease[1]. This projection became known as Moore's Law. It set the electronics industry on a quest for continued scaling for more than 50 years and those who have mastered the technology have enjoyed the greatest commercial benefits and the greatest gains in defense capabilities. However, it is clear that the design work and fabrication now required to keep pace is becoming increasing difficult and expensive. The current trajectory of scaling has strained both the commercial and defense sectors, as much for economic as for technical reasons.

From a national security perspective, the dynamics that resulted from Moore's observations and analysis have become increasingly complex. The Department of Defense (DoD) has ridden the relentless wave of technical progress in electronics to create exceptionally complex and high-performance systems. However, the current cost of development is challenging the national security enterprise. The rate of development of novel and unique electronics, based on advances in fundamental science and engineering research, has dwindled within the DoD. The number of leading-edge manufacturing sites that are considered a part of the national security enterprise is diminishing, and the fundamental tie between national security and the health of the electronics industry is strained. The shift in focus of all major electronics entities has been towards large-volume global supply chains as a means to manage the dynamics and economics of scaling. But this has also made it more difficult for the DoD to leverage industry capabilities for the small-volume, high-performance technology that the defense sector needs. With the Electronics Resurgence Initiative (ERI), DARPA seeks to address these imbalances, ultimately working hand-in-hand with industry to embrace the coming inflection in Moore's Law. The goal of the ERI is to more constructively enmesh the technology needs and capabilities of the defense enterprise with the commercial and manufacturing realities of the electronics industry.

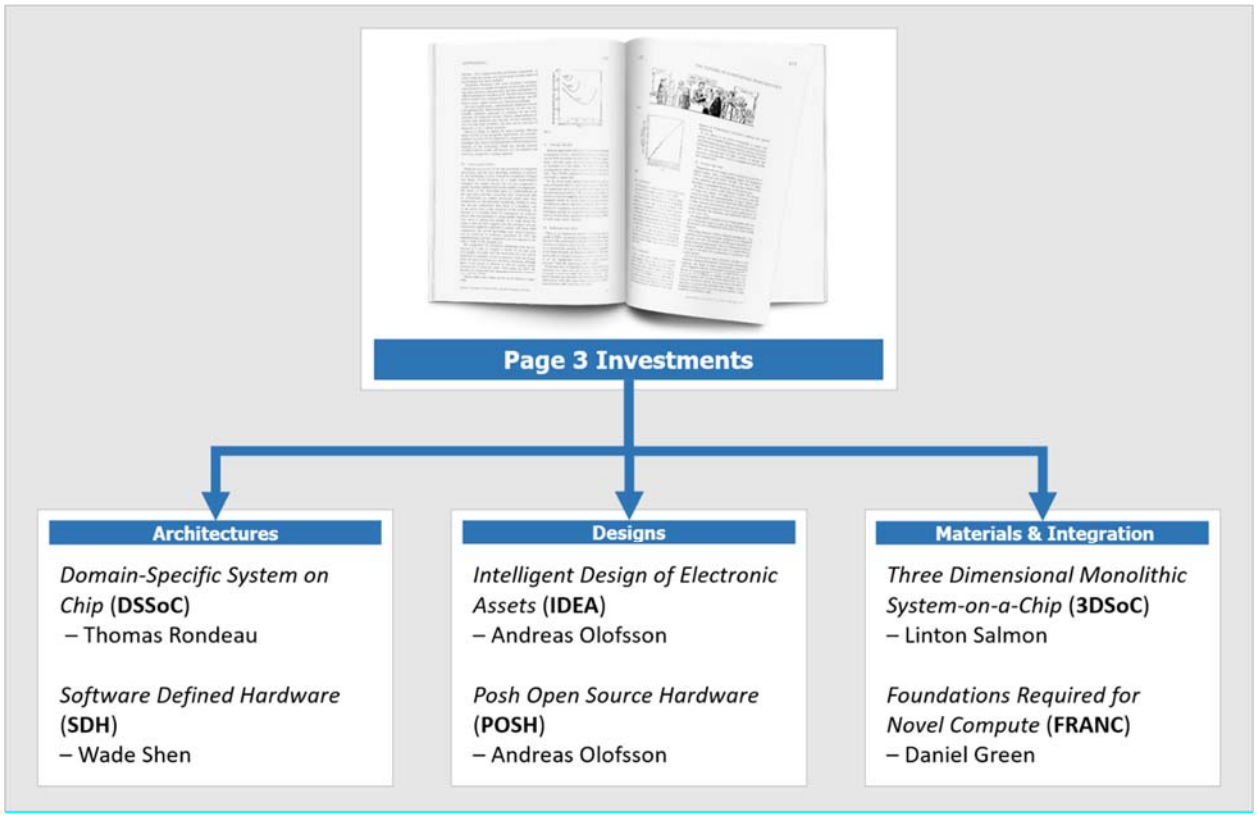
[1] G. E. Moore, "Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp.114," in Proceedings of the IEEE, vol. 86, no. 1, pp. 82-85, Jan. 1998. doi: 10.1109/JPROC.1998.658762 <https://doi.org/10.1109/JPROC.1998.658762>



Electronics Resurgence Initiative (ERI)

During these unique times, it is instructive to read all of Moore's prescient paper. On page two, he laid out what became his famous projection for scaling transistor count. However, on page three, with an eye toward the times we now live in, he laid out the technical directions to explore when the conditions under which scaling will be the primary means for advancement are no longer met. A trio of simultaneously-released ERI BAAs—this one among them—parallel the research areas detailed on page three of Moore's paper: materials and integration, architecture, and design. These new page-three-inspired investments, along with a series of related investments from the past year, comprise the overall Electronics Resurgence Initiative.

The "ERI Page 3 Investments" are the next steps in creating an electronics capability that will provide a foundational contribution to U.S. national security. They reflect a collaborative spirit that we hope will lead an electronics industry capable of meeting its own commercial needs and ambitions while simultaneously advancing national defense in the 2025 to 2030 time frame. DARPA is eager to receive proposals from entities that can further the broader cause of the electronics industry while simultaneously embracing national security, based on the development and consistent availability of advanced, high-performance electronics technologies.



ERI Page 3 Investments Overview

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PART I: OVERVIEW INFORMATION

- **Federal Agency Name**: Defense Advanced Research Projects Agency (DARPA), Microsystems Technology Office (MTO)
- **Funding Opportunity Title:** Electronics Resurgence Initiative: Page 3 Design
- **Announcement Type:** Initial Announcement
- **Funding Opportunity Number:** HR001117S0054
- **Catalog of Federal Domestic Assistance Numbers (CFDA):** 12.910 Research and Technology Development
- **Dates:** (All times listed herein are Eastern Time)
  - Posting Date: September 13, 2017
  - Proposers Day: September 22, 2017
  - FAQ Submission Deadline: 1:00 PM on November 1, 2017
  - Proposal Due Date: 1:00 PM on November 14, 2017
  - Estimated period of performance start: May 2018

Concise description of the funding opportunity:
DARPA is soliciting innovative research proposals in the area of physical design of electronic circuits and systems. Proposed research should investigate innovative approaches that enable revolutionary advances in science, devices, or systems.

The Design thrust of the Electronics Resurgence Initiative (ERI): Page 3 Investments will address today's System-On-Chip (SoC) design complexity and cost barriers, creating the environment needed for the next wave of US semiconductor innovation. Programs within this thrust will develop the algorithms and software required to realize a unified layout generator that will enable fully automated "no human in the loop" physical design of SoCs, system-in-packages (SiPs), and printed circuit boards (PCBs) in 24 hours. In parallel, programs will create the building blocks, validation methodologies, and infrastructure required for a scalable open source hardware ecosystem, bringing best practices in software to hardware design.

- **Anticipated individual awards**: Multiple awards are anticipated
- **Anticipated funding type:**
  - IDEA: 6.1 and 6.2
  - POSH: 6.2
- **Types of instruments that may be awarded:** Procurement contract, grant, cooperative agreement or other transaction.
- **Agency contact:**
  - Andreas Olofsson, Program Manager
    BAA Coordinator: HR001117S0054@darpa.mil
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    675 North Randolph Street
    Arlington, VA 22203-2114

PART II: FULL TEXT OF ANNOUNCEMENT

I. Funding Opportunity Description

The Defense Advanced Research Projects Agency (DARPA) often selects its research efforts through the Broad Agency Announcement (BAA) process. This BAA is being issued, and any resultant selection will be made, using the procedures under Federal Acquisition Regulation (FAR) 6.102(d)(2) and 35.016 and 2 C.F.R. § 200.203. Any negotiations and/or awards will use procedures under FAR 15.4, Contract Pricing, as specified in the BAA (including DoDGARS Part 22 for Grants and Cooperative Agreements, and Part 37 for Technology Investment Agreements). Proposals received as a result of this BAA shall be evaluated in accordance with evaluation criteria specified herein through a scientific review process.

DARPA BAAs are posted on the Federal Business Opportunities (FedBizOpps) website, http://www.fbo.gov/, and, as applicable, the Grants.gov website at http://www.grants.gov/. The following information is for those wishing to respond to the BAA.

The Microsystems Technology Office at DARPA seeks innovative proposals in the areas of physical design and verification that will enable rapid specialization of SoCs. It is anticipated that research with the Electronic Resurgence Initiative Design thrust will create modular software for completely automated physical design of electronic circuits and an open source hardware ecosystem through creation of open source “Intellectual Property” circuit and validation technology. Research within this program is expected to drastically reduce the cost and design time of PCBs, SiPs, and integrated circuits. Proposed research should investigate innovative approaches that enable revolutionary advances in science, devices, or systems.

A. Background

Next-generation intelligent systems supporting Department of Defense (DoD) applications in artificial intelligence, autonomous vehicles, shared spectrum communication, electronic warfare, and radar will require processing efficiency orders of magnitude better than what is offered by current commercial electronics. Reaching the performance levels required by our Nation’s needs will require development of highly complex SoC platforms leveraging the most advanced integrated circuit technologies. Unfortunately, as the complexity of chips has rapidly increased in line with Moore’s law predictions, recent years have seen an explosion in the cost and time required to design advanced SoCs, PCBs, and SiPs, as illustrated in Figure 1. To fully unlock innovation and maintain the DoD’s technical superiority, the Page 3 Design thrust will develop new paradigms for intelligent physical design and reduce the barriers to design of high-performance, high-efficiency custom integrated circuits.

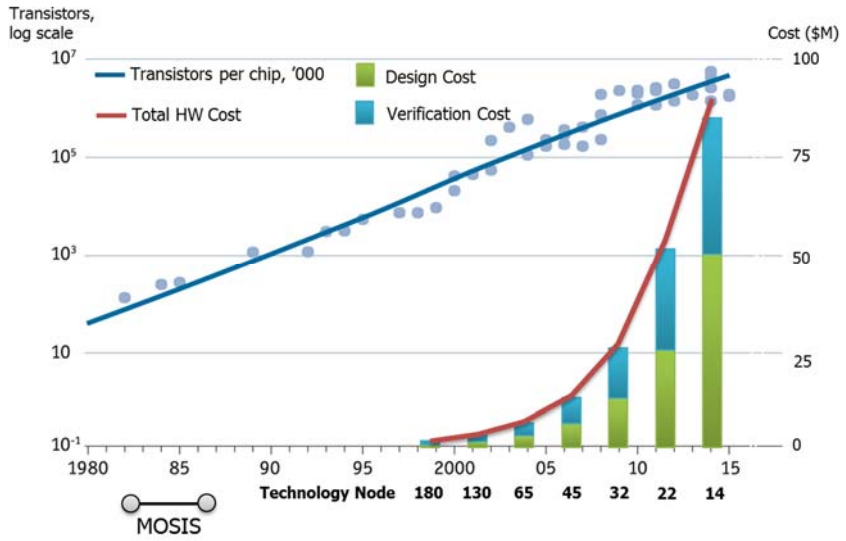

Figure 1. Illustration of the rapid increase in resources required for physical design and verification as Moore's Law has progressed.

The barriers facing the physical design of integrated circuits today parallel some of the challenges faced by chip designers nearly three decades ago. At that time, high costs and difficult access associated with chip fabrication presented a severe bottleneck to prototyping of novel circuits and designs by research institutions. To remove the fabrication barriers that were inhibiting semiconductor innovation, DARPA developed the Metal Oxide Semiconductor Implementation Service (MOSIS) program. MOSIS enabled cost-effective prototyping of chips through multi-project wafer runs. Supported by strong industry demand, the successful MOSIS program launched the fabless electronics industry and led to a wave of US semiconductor innovation.

Like MOSIS, the Page 3 Design thrust will foster the environment needed for the next wave of U.S. semiconductor innovation. Through creation of a software-based, "no human in the loop" physical layout generator and an open source Intellectual Property (IP) eco-system, the Page 3 Design thrust will usher in an era of 24-hour design for DoD hardware systems, shorten upgrade cycles, and enable wide proliferation of commercial and DoD-specific SoCs. The Page 3 Design thrust will encompass two programs, the Intelligent Design of Electronic Assets (IDEA) and Posh Open Source Hardware (POSH).

B. Page 3 Design Description

The Page 3 Design thrust includes two programs that will operate independent of each other:

- **Intelligent Design of Electronic Assets (IDEA):** "No human in the loop" 24-hour layout generation for mixed signal integrated circuits, systems-in-package, and printed circuit boards.
- **Posh Open Source Hardware (POSH):** An open source System on Chip (SoC) design and verification eco-system that enables cost effective design of ultra-complex SoCs.

When proposing to multiple programs, proposers are required to propose solutions for IDEA and/or POSH in separate proposals. **Proposers should not propose to more than one program in a single proposal.** Further information about the programs can be found in Section C (IDEA) and Section D (POSH).

C. The Intelligent Design of Electronic Assets (IDEA) Program

1. Program Background

Today's typical physical design flow consists of multiple phases implemented by moderate to large teams of physical designers using Computer Aided Design (CAD) tools as aids to perform chip floor-planning, device placement, routing, and physical verification. Despite commonalities between design flow steps in integrated circuits (ICs), SiPs, and PCBs, layout is completed using separate tools by design groups with minimal overlap. In the digital IC domain, layout automation has been integral to the design of complex circuits at advanced technology nodes, but progression towards full automation has now stalled. In the analog and board domains, physical design is still a largely manual process, preventing cost- and resource-efficient layout of truly complex mixed signal systems. Commercial electronics manufacturers of SoCs employ large teams of designers, each with expertise in a specific facet of the design flow to meet design requirements; however, DoD researchers and development teams do not have the resources available to effectively execute such a strategy, resulting in hardware design cycles of 12-36 months.

To overcome these limitations and keep pace with the exponential increases in SoC complexity associated with Moore's law, the IDEA program aims to develop a fully automated "no human in the loop" circuit layout generator that enables users with no electronic design expertise to complete physical design of electronic hardware.

As shown in Figure 2, the IDEA layout platform will support automated physical layout of multiple types of electronic components, including analog and digital SoCs, SiPs, and PCBs. IDEA will develop the infrastructure, algorithms, methods and software required to successfully demonstrate "no human in the loop" physical layout, transforming a complete design netlist into a manufacturable layout database. It is envisioned that the IDEA platform will leverage applied machine learning methodologies to continuously evolve and improve performance as new data sets become available. The customization offered from training will empower differentiation through the breadth and quality of training sets available to the end user, providing specialized users with an asymmetric advantage benefiting from an existing database of designs. Through 100% automation of electronics layout, IDEA is expected to usher in a new era of 24-hour design of DoD hardware systems. It is anticipated that achieving the autonomy goals of the IDEA program will require breakthroughs in machine learning and optimization algorithms.

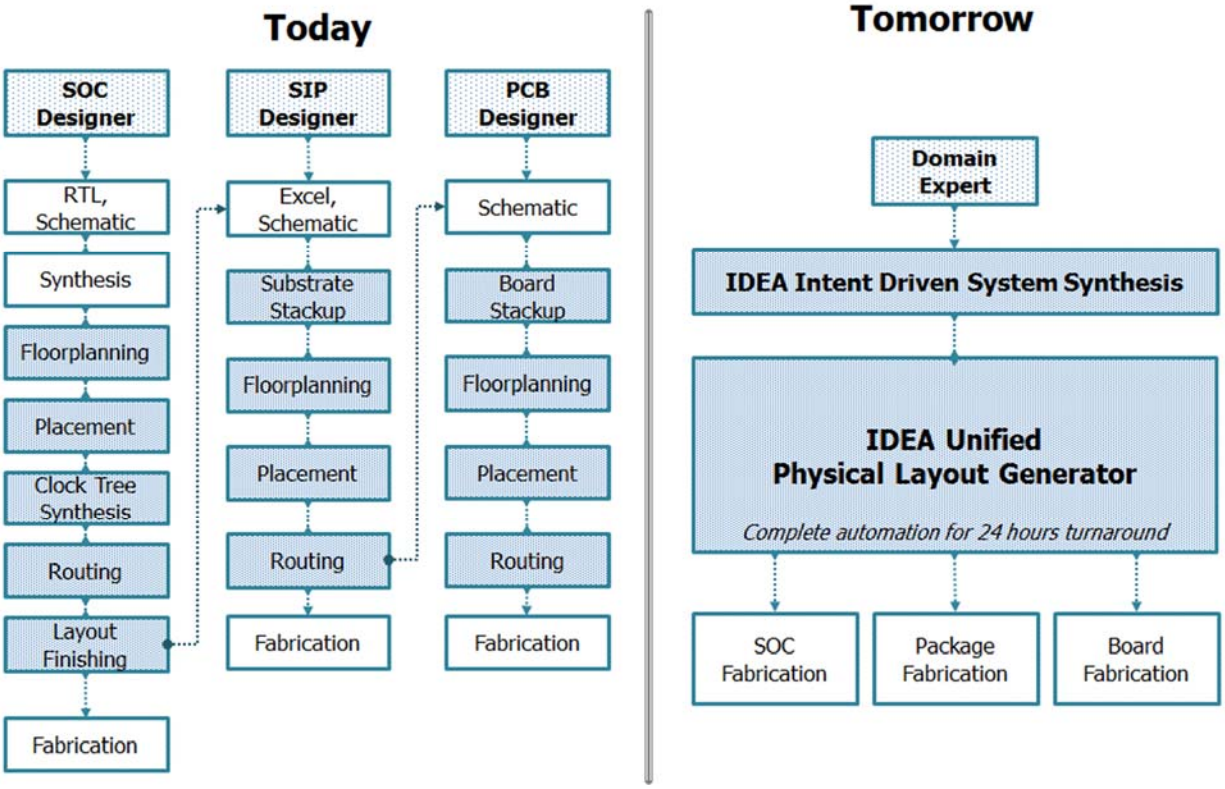

Figure 2. Illustrative design flow describing existing design practices and the components of physical layout that the IDEA unified physical design generator will complete.

2. Program Structure

The IDEA program includes two main Technical Areas (TAs). The Technical Areas are illustrated in Figure 3 and are described below:

TA-1: Machine Generated Physical Layout: Development of a unified physical layout generator for digital and analog SoCs, SiPs, and PCBs.

TA-2: Intent Driven System Synthesis: Development of an intent-driven, correct-by construction system generator.

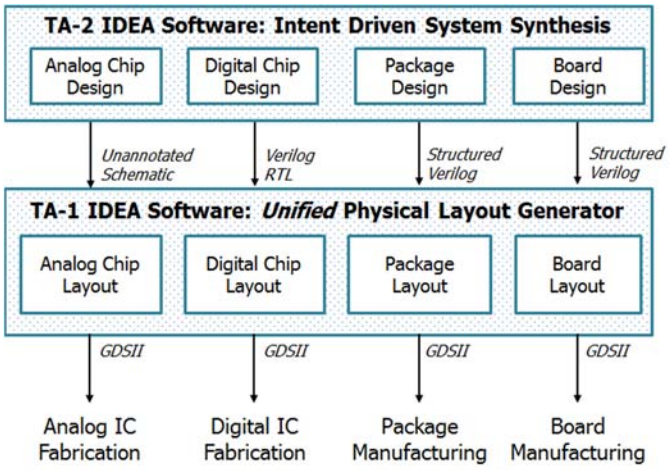

Figure 3. A flowchart providing a high-level illustration of the IDEA technical areas. The figure indicates the formats the software is expected to support for digital and analog SoC, SiP and PCB physical design.

IDEA does NOT seek proposals for:

- Investigatory research that does not deliver useful software
- Development of high level languages, compilers, and generators for Boolean logic design
- Architectures that simply reduce or remove the need for physical layout
- New manufacturing processes and technologies

Each technical area will contain multiple subtasks to which performers may propose solutions. Proposals that address more than one IDEA technical area or multiple subtasks within a technical area must be constructed so that each subtask can be selected independently from one another. Proposers who include multiple subtasks in their proposal should describe each subtask separately and should provide separate pricing for each subtask.

Due to the complexity of physical design, it is anticipated that performers will be developing software modules for individual portions of the design flow and working with other performers to create a complete IDEA TA-1 or TA-2 software design flow meeting the IDEA program metrics. Close coordination among performers in all technical areas will be critical to program success. Performers not proposing a complete solution will be required to collaborate with other performers and integrate modules into the software platform continuously throughout the program.

Integration exercises, one week in length, will be held twice a year in each phase for software integration and evaluation of the "no human in the loop" physical layout and system generators. All IDEA performers will be required to attend and work with other performers during these integration exercises. Performers are also expected to adapt proposed algorithms and modules throughout the program to continuously optimize the performance of the unified physical layout generator and system generator. Given the importance of open interfaces and interoperability between software modules, proposals must include a one page long Collaborative Statement that describes (1) how the proposed work will be integrated within the IDEA design flow, (2) performer's prior experience with open collaboration, (3) a declaration of any license and copyright restrictions imposed on the delivered software and intra-module Application Programming Interfaces (API), and (4) an affirmation, indicated by signature on the Collaborative

Statement document, that the proposer accepts the requirement to collaborate with other program performers as necessary to meet the overall program goals and objectives stipulated in the BAA and the proposer's Statement of Work (SOW).

Program evaluation will be conducted by U.S. Government (USG)/Federally Funded Research and Development Centers (FFRDC) personnel. The evaluation effort will consist of physical design of a suite of government provided SoC, SiP, and PCB benchmarks and comparison of the power, performance and area against a physical layout completed using traditional techniques. Evaluations will be conducted throughout each phase and at each integration exercise. Performers may continue from Phase 1 to Option Phase 2 based on software modification in response to technical feedback, evaluation at integration exercises, and end-of-phase evaluations conducted on the integrated software platform.

In addition to novel research, the program will emphasize delivery of working high quality software. Software modules created in the program are expected to be interoperable with modules developed by other program performers, and intellectual property rights asserted by proposers are strongly encouraged to be aligned with non-viral open source licenses such as the Apache 2.0, Massachusetts Institute of Technology (MIT), and Berkeley Software Distribution licenses. If a proposed approach includes proprietary software or technical data as a component of the approach, the proposer is expected to provide 1) clear justification for the need for the proposed software, and 2) a description of how the IDEA program goals will be met with use of the proprietary model.

3. TA-1: Machine Generated Physical Layout

The primary goal of IDEA TA-1 is to create and deliver a *unified platform* for completely automated layout generation of SoCs, SiPs, and PCBs. A notional IDEA layout generator framework is shown in Figure 4 and defines the critical design steps of the design flow from source input to physical deliverable. Proposers should note that the notional design flow architecture is provided for clarification and is expected to evolve over the course of the program. Performers may propose to develop automated software for one, multiple, or all identified subtasks, with the expectation that software modules will be integrated into the complete software platform throughout the program. IDEA TA-1 also encourages proposals from analog and digital design teams that will develop novel SoC designs and interact with TA-1 software developers to support evaluation of the IDEA physical design platform.

The critical research questions for this technical area are:

- Can we achieve "no human in the loop" SoC, SiP, and PCB layout at advanced nodes?
- To achieve "no human in the loop" layout, what power, performance, area (PPA) results should be targeted?
- Can we demonstrate a layout platform that continuously improves with additional data from new designs and training sets?
- What algorithms and machine learning techniques are best suited to achieving the goal of "no human in the loop" automation?

- What design and CAD approaches are scalable to supercomputer and data-center size compute infrastructure?
- What design methodologies and design infrastructure are needed for fully automated layout?
- How can we completely decouple front end design details and EDA flows from proprietary foundry rules and models, such as process development kits (PDKs)?

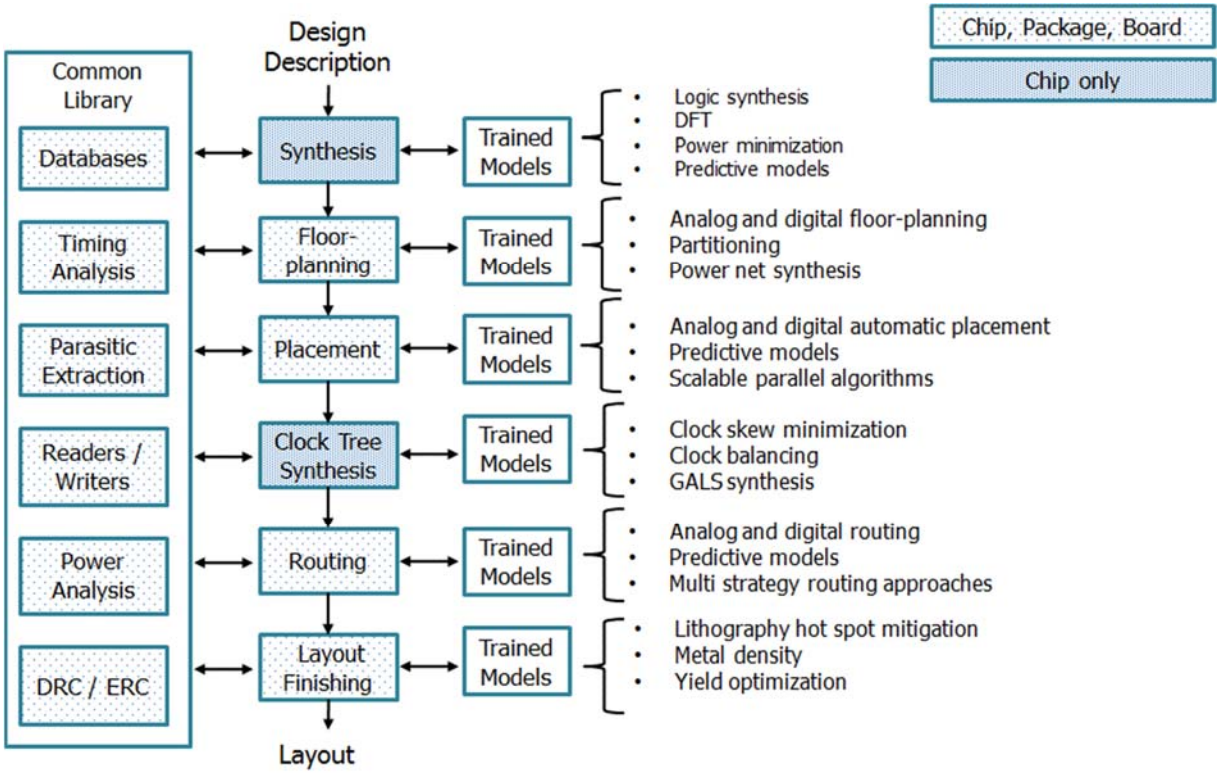

Figure 4. A description of the notional IDEA TA-1 software framework, illustrating critical design flow subtasks and an outline of key characteristics. TA-1 performers may propose to develop software for some or all of the identified subtasks. The image is color coded to indicate whether the proposed software for the specified subtask must be applicable to chips only, or chips, boards and packages.

The software developed in IDEA TA-1 is expected to take standard design source files as inputs and produce complete GDSII databases ready for manufacturing. Specifically, the software platform is expected to produce complete layout databases using one or more of the following inputs: (1) unannotated netlists for analog IC designs, (2) Verilog Register Transfer Level (RTL) and instantiated fixed circuit primitives/macros circuit blocks for digital IC designs, and (3) structured Verilog netlists for SiPs and PCBs. The software platform will be evaluated against novel designs created by SoC designers as well as the government benchmark suite.

The overarching goal of TA-1 is to create a unified software platform capable of continuous improvement through training and experience that meets the program metrics as identified in Table 1. It is anticipated that development of such a platform will be an extensive collaborative endeavor, and program performers may propose to develop software modules for portions of the design flow

that will be integrated into the final software platform. In addition to novel research, all TA-1 performers will be required to work collaboratively to define the required standards, open interfaces, and design methodology needed to build a seamless, publicly releasable platform for layout generation of SoCs, SiPs, and PCBs. Performer software modules will be evaluated both individually and as part of the physical layout generator platform. TA-1 deliverables will be verified through layout of a set of openly available government furnished benchmark circuits. The following list gives an indication of the types of benchmarks that may be included in the government furnished benchmark suite:

- OpenPiton (http://parallel.princeton.edu/openpiton/#infosec)
- RISC-V Rocket chip (https://github.com/freechipsproject/rocket-chip)
- BeagleBone (https://beagleboard.org/black)
- Facebook Wedge Board (https://opencompute.org)
- BaseJump Wirebond Ball Grid Array (BGA) package (http://bjump.org/)

Table 1. TA-1 metrics by phase. Relative PPA is PPA referenced to SoC benchmarks created with traditional design flow techniques.

Technical Area	Metrics	Phase 1	Phase 2
IDEA TA-1: Machine Generated Physical Layout	SoC Benchmarks	Government furnished benchmarks 14nm CMOS PDK	Government furnished benchmarks 7nm & 14nm CMOS PDK
	Board Benchmarks	BeagleBone Black[1]	Open Compute Server[2]
	SiP Benchmarks	Government furnished benchmarks	Government furnished benchmarks
	Benchmark $PPA_{IDEA}/PPA_{Traditional}$[(3)]	0.5	1
	Package Complexity	Up to 2 die, 2.5D	Up to 1024 die, 2.5D
	Automation	100%	
	Turnaround time	24 hours	
	Deliverable	Software, license[4], software documentation	

[1]This metric is a measurement of functional equivalence to a BeagleBone Black circuit card.
[2]This metric is a measurement of functional equivalence to an Open Compute Server.
[3]Relative Power, Performance, Area (PPA) as compared to benchmark layout completed by a small physical design team using off-the-shelf tools current to 2017 commercial EDA ideology. Higher numbers indicated higher quality with "1" being the current status.
[4]Delivered with a minimum of government purpose rights; open source licenses are preferred.

The physical layout generator developed in TA-1 is expected to support existing state of the art design techniques, including but not limited to:

- Analog, digital, and mixed signal design
- Asynchronous and synchronous digital design styles

- Clock gating
- Automated pipeline retiming
- Multiple clock domains
- Multiple voltage domains
- Power gating and adaptive voltage scaling
- Scan insertion
- Physical design hierarchy
- Large designs (>100M placed instances)
- Flip-chip, micro-bumps, and wire-bond packaging
- 2.5D Systems-in-Package
- Advanced PCB manufacturing technologies, consistent with technologies used for 2017 smartphone manufacturing

Phase 1: Exploratory Research [Base – 24 months]
In Phase 1 of TA-1, performers are expected to develop new concepts and collaborate with other TA-1 performers to create and integrate software modules into a completely automated layout generator that achieves 50% of the PPA target of existing human-centric EDA flows. This includes:

1. Codifying state of the art designer knowledge
2. Demonstrating pathways to apply machine learning to physical design and creation of annotated datasets for machine learning
3. Collaborating on IDEA standards and APIs
4. Developing software modules within the IDEA automated layout generation pipeline
5. Delivering alpha, beta and public versions of modules developed in Phase 1 for completely automated back-end physical design. Software should support physical design at multiple technology nodes, including 14nm, 28nm, 65nm, and 180nm CMOS.

Phase 2: Optimization and System Demonstration [Option – 24 months]
In Phase 2 of TA-1, performers should extend concepts developed during Phase 1 with the goal of reaching a performance of 100% PPA compared to existing resource limited human-centric design flows used to layout the benchmark circuits provided by the USG/FFRDC. This includes:

1. Advancing the state of the art in machine learning to leverage a diverse set of strategies and algorithms to optimize performance on a per circuit basis.
2. Extending module applicability to support newer CMOS technology nodes, including 7nm, while maintaining applicability to 14nm, 28nm, 65nm, and 180nm nodes.
3. Training the physical design platform on expanded datasets and redesigning Phase 1 benchmark circuits at 14nm node to demonstrate PPA improvements achieved through additional learning.

4. Delivering stable versions of the IDEA software modules appropriate for large user scale deployment.
5. Increasing the number of IDEA platform users to ensure successful software transition at the end of the program.

A list of the TA-1 subtasks that proposers are encouraged to address is provided in Table 2. Proposers are expected to develop or use existing data to create the required training models; data will not be supplied by the USG/FFRDC. Unless otherwise specified in the Description column of Table 2, proposed solutions are expected to support analog and digital SoCs, SiPs and PCBs. For example, a proposed solution for an automated routing software module should support routing for digital ICs, analog ICs, SiPs and PCBs; a proposed automated router that only supports digital IC design is not within scope. If a proposal addresses a design step not identified in Table 2, a thorough technical justification must be provided discussing the need for the module and relevance to successful creation of an automated physical design flow.

Table 2. Table identifying and describing subtasks proposers may propose to as part of IDEA TA-1. Performers may propose solutions for one or multiple of the identified subtasks.

	TA-1 Subtask	Description
Common Infrastructure	**Databases / Processing**	Create critical infrastructure for TA-1 performers, including but not limited to: distributed and in-memory design databases, infrastructure for distributed EDA computing on data-center and supercomputer scale computers.
	Cloud infrastructure	Develop compute infrastructure, IP firewalling, and merchant eco-system needed to allow the "no human in the loop" IDEA layout generator to be effectively accessed as a cloud based software service by the broader community.
	Timing Analysis	Full circuit and incremental scalable timing analysis software for synchronous and asynchronous circuits. Interacts with synthesis, floorplanning, placement, clock-tree synthesis, routing, and layout finishing sub-tasks through an open API.
	Parasitic Extraction	Extraction technology, foundry-specific parasitic models for capacitance, resistance, inductances. Interoperable with all TA-1 software modules.
	Readers + Writers	Optimized parsers, readers, writers for standard file formats such as Verilog, GDSII, LEF, DEF, SPICE, LIBERTY, SDC, and PDKs.
	Power and Signal Integrity Analysis	Circuit power and signal integrity software with support for instantaneous dynamic power analysis, static power consumption, electro-migration, reliability, and thermal analysis. Interacts with synthesis, floorplanning, placement, clock-tree synthesis, routing, and layout finishing sub-tasks through an open API.
Layout Generators	**Logic Synthesis**	Transform Verilog RTL to a gate level netlist (digital circuits only).
	Floor-planning	Generate correct by construction floor-plans using structured netlists, PDK, minimal user constraints, and trained models as inputs.
	Placement	Place all cells/parts using floorplan, structured netlist, PDK, minimal user constraints, and trained models as inputs.
	Clock Tree Synthesis	Synthesis and layout of a clock distribution network (digital circuits only).

	Detailed Routing	Route all nets in the design using placed circuit, PDK, minimal user constraints, and trained models as inputs.
	Layout Finishing	Design For Manufacturing optimizations using routed circuit, PDK, minimal constraints, and trained models as inputs.
Design	**SoC Design Advisors**	Expert design teams that will act as advisors to the IDEA layout platform developers and use the IDEA software to demonstrate "no human in the loop" layout of an appropriate 100mm^2 SoC at 14nm CMOS as well as accompanying package and board.

TA-1 performers will be encouraged to build software in a modular fashion and are expected to utilize standard read/write formats to ensure interoperability. Proposers should describe a strategy for contribution and maintenance of their software modules on an accessible platform and growth of the user community within the integrated software platform in their proposal. Performers will be encouraged to create repositories open to program collaborators and frequently release software modules developed throughout IDEA on an industry-standard, accessible software collaboration platform.

Also included in Table 2 is a subtask encouraging proposals from analog and digital design teams, "SoC Design Advisors", to support the evaluation of the IDEA back-end physical design platform. The Design Advisors are expected to design novel high performance SoCs for an identified application and use the IDEA platform to complete physical design of the SoC and associated package and board. Proposers should identify the application and pathways to performance improvement over today's state of the art in the proposal. Proposers should leverage the wide variety of designs the IDEA platform will support, including analog and digital circuits and next generation packaging formats. DARPA will provide fabrication support for proposers to the SoC design team subtask through a number of separately funded multi-project or dedicated wafer runs; therefore, fabrication costs should not be included in proposal budgets. As shown in Figure 6, proposers should assume an early Phase 2 tapeout will occur at a primary commercial foundry at the 14nm CMOS technology node and a later Phase 2 tapeout will occur at a primary commercial foundry at the 7nm CMOS technology node. Teams proposing to SoC Design Advisors will be expected to deliver SoC, packaging and board hardware at the end of Phase 2.

A selectable proposal for one or more subtasks of the IDEA TA-1 framework must include the following:

- A description clearly stating whether the proposed software module supports a step in the IDEA design framework identified in Table 2
- A description of the unique technical merits and value provided by the technology to meet the goals of the TA-1 as described above. Proposers may use prior work to argue the technical merits of their approach
- A description of each proposed software module and its function
- A description of how proprietary PDK related data will be separated from the main layout generator and how communication with said model is handled.

- A description of 1) the data the training models will be extracted from and 2) how proprietary trained "knowledge models" will be separated from the main layout generator and how communication with said model is handled.
- A list of constraints for the software module, identifying the source of the constraints (whether from other software module or initial user input)
- A full description of required design inputs, where applicable
- A full description of design outputs, where applicable
- A discussion of the plan to achieve autonomous functionality for the software module in the following regards:
    - Autonomous operation – given inputs and constraints, produce output without human intervention
    - Autonomous handoff – condition outputs such that they can be used by other modules without human intervention
- A description of the proposer's anticipated software release schedule
    - Public releases of software are required at the end of each phase
    - At a minimum, controlled releases should occur on an industry-leading collaborative development platform prior to each scheduled integration exercise. Additional releases to facilitate integration are strongly encouraged
- A description of appropriate mid-phase technical metrics applicable to the evaluation of the proposed software modules

4. TA-2: Intent Driven System Synthesis

Given a high-level functional description and minimal constraints, the software developed in IDEA TA-2 will create correct-by-construction PCBs and systems based on a vast library of Commercial Off The Shelf (COTS) components. Examples of COTS components include commercially available packaged chips for PCBs, bare die for SiPs, and IP modules for SoCs. The design netlist created by the TA-2 software will be fed into the layout generator developed in TA-1 to create an end-to-end automated design platform for PCBs, SoCs and SiPs.

Today's design of complex systems is a largely manual process involving the following steps:

1. Creation of a text document describing functional specifications, power, area, performance, reliability, and cost constraints
2. Selection of a perceived optimal set of devices from a rich library of existing parts
3. Manual design of exact electrical schematic using said parts
4. Placement of components and routing of all nets and power connections
5. Manual review and simulation (optional)

IDEA TA-2 seeks to create software to replace steps 1-3 of the process above, while TA-1 creates automated software for step 4.

While purely Boolean circuits can be realized from a finite library of well understood combinatorial and sequential cells, complex PCB and SoC designs are realized from a much larger library of complex components, most of which cannot be represented by a simple mathematical model. Currently, there are over five million commercial COTS parts in circulation, with component descriptions embedded in text data sheets that require manual review, leaving no path to automated parts selection with a system generator.

A notional design flow architecture for IDEA TA-2 is illustrated in Figure 5. Proposers should note that the notional design flow architecture is provided for clarification and is expected to evolve over the course of the program. As illustrated, the backbone of the design flow is supported by creation of an open parts database with an extensive library of components to meet the extreme needs of the DoD. Performers may propose to develop automated software for one, multiple, or all identified subtasks, with the expectation that software deliverables will be integrated into the complete TA-2 software platform throughout the program. If a performer proposes a different design flow or a design step not identified in Figure 5, a thorough technical justification must be provided detailing why the module is required for successful creation of an intent driven system design platform for PCBs, SoCs and SiPs. Performers within each subtask are expected to work together and collaboratively develop the models required for the platform.

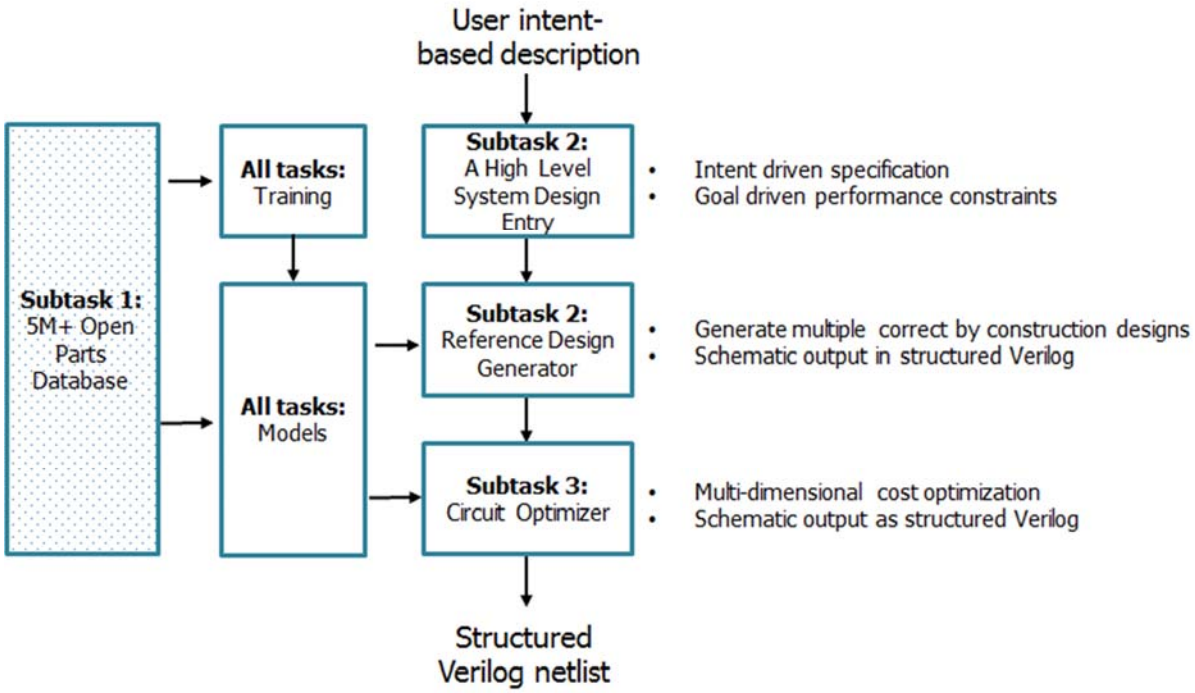

Figure 5. A notional design flow illustrating the IDEA TA-2 subtasks: 1) an open parts database, 2) a system generator consisting of high level system design entry and a reference design generator, and 3) a circuit optimizer.

The TA-2 technical work consists of three sub-tasks:

1) 5M+ Open Parts Database: Development of an expansive library (with the capacity to support data for more than five million entries) of appropriately modeled COTS parts

supporting PCBs, SiPs and SoCs for use by the schematic generator and optimization tools developed in IDEA TA-2. The library should support a large diversity of components including, but not limited to, microcontrollers, DRAM, ADCs, DACs, PMICs, IO interfaces, passive devices and connectors. It is anticipated that this task will involve automated data mining of the large corpus of open datasheets and documentation associated with COTS parts currently in distribution.

2) System Generator: Creation of methodologies for high level system design entry, and development of a system generator that creates a selection of known good structured Verilog netlists based on user provided intent-based descriptions.
3) Circuit Optimizer: Development of a circuit optimizer that takes structured generic Verilog netlists as an input and produces an optimized design based on criteria such as size, weight, power, cost, reliability, and system standard compliances.

IDEA TA-2 performers will be required to work with other performers in TA-2 to define the required set of standards, open interfaces, and techniques necessary to build seamless, publicly releasable software necessary to meet the TA-2 program metrics specified in Table 3. Performer software modules will be evaluated both individually and as part of the physical layout generator platform. TA-2 deliverables will be verified through layout of the benchmark boards specified in Table 3.

Phase 1: Exploratory Phase [Base – 24 months]
In the exploratory phase of TA-2, performers are expected to demonstrate new concepts and work with other TA-2 performers to create a complete high-level system synthesis platform for SoCs, SiPs and PCBs. Within Phase 1, performers are expected to:

1. Develop architecture, concepts and requirements for intent-driven system generators.
2. Develop and deliver automated software required for high-level synthesis, including reference design generators, intent-driven synthesis, high-level system design entry, and automated COTS part database creation.
3. Identify parts library modeling requirements based on the needs of the system generator and circuit optimization tools. Create methods for extracting model information from elements added to the Open Parts database.
4. Create a vast library of COTS parts modeled using extended IC formats such as GDSII, LEF, LIBERTY, IP-XACT. At a minimum, the library should include all parts needed design the Phase 1 benchmarks, as identified in Table 3. Proposers are encouraged to create fully automated data mining and model technology to enable automated model creation for close to all 5M+ open parts in circulation.
5. Utilize existing commercial PCB layout tools to create physical layouts of the structured netlists created by the IDEA TA-2 generators in preparation for manufacturing early in Phase 2.

Phase 2: Optimization and System Demonstration [Option – 24 months]
In Phase 2, performers are expected to:

1. Manufacture boards designed in Phase 1 using the IDEA system synthesis platform and traditional physical layout tools.
2. Integrate the front-end system generator software created in Phase 1 of TA-2 with the physical layout generator created by TA-1 and produce a fully automated end-to-end electrical system generator.
3. Manufacture and deliver boards designed with the fully automated end-to-end electrical system generator.
4. Actively optimize software and documentation to enable adoption by a large number of new users to ensure successful software transition at the end of the program. Models library developers should continue adding elements to the Open Parts Database, and demonstrate successful use of the model library within the design flow.

Table 3. TA-2 metrics by Phase.

Technical Area	Metrics	Phase 1	Phase 2
TA–2: Intent Driven System Synthesis	SoC Benchmark	SoC with 10 IPs	SoC with 100 IPs
	PCB Benchmark	BeagleBone Black[1]	Open Compute Board[2]
	SiP Benchmark	Establish pathway to SiP generation	Demonstrated fully automated layout of SiPs with >100 chiplets and >100,000 nets
	Benchmark $PPA_{IDEA}/PPA_{Traditional}$[(3)]	0.5	1
	Automation	100%	
	Turn around time	24 hours	
	Deliverable	Software, license[4], documentation	

[1]This metric is a measurement of functional equivalence to a BeagleBone Black circuit card.
[2]This metric is a measurement of functional equivalence to an Open Compute Server.
[3]Relative Power, Performance, Area as compared to benchmark design completed by a small physical design team using off-the-shelf tools current to 2017 commercial EDA ideology. Higher numbers indicated higher quality with "1" being the current status.
[4]Delivered with a minimum of government purpose rights; open source licenses are preferred.

A selectable proposal for one or more subtasks of the IDEA TA-2 framework must include the following:

- A description clearly stating whether the proposed software module supports a step in one of the three sub-tasks identified in TA-2
- A description of the unique technical merits and value provided by the technology to meet the goals of IDEA TA-2 as described above. Proposers may use prior work to argue the technical merits of their approach.
- A description of each proposed software module and its function

- A description of how proprietary trained "knowledge models" will be separated from the main system generator and how communication with said model is handled.
- A list of constraints for the software module, identifying the source of the constraints (whether from other software module or initial user input)
- A full description of required design inputs, where applicable
- A full description of design outputs, where applicable
- A discussion of the plan to achieve autonomous functionality for the software module in the following regards:
    - Autonomous operation – given inputs and constraints, produce output without human intervention
    - Autonomous handoff – condition outputs such that they can be used by other modules without human intervention
- A description of the proposer's anticipated software release schedule:
    - Public releases of software are required at the end of each phase
    - At a minimum, controlled releases should occur on an industry-leading collaborative development platform prior to each scheduled integration exercise. Additional releases to facilitate integration are strongly encouraged
- A description of appropriate mid-phase technical metrics applicable to the evaluation of the proposed software modules

5. Schedule and Milestones

The IDEA program schedule comprises a 24-month base period (Phase 1) followed by a 24-month option period (Phase 2), for a total of 48 months, subject to availability of funds and technical progress achieved. Due to the likelihood that performers will be developing individual modules of a software platform, proposers will be required to establish intermediate goals and milestones that support their strategies.

Performers will be assessed throughout the program based on their individual technical progress as well as the performance of the full IDEA software platform against the program metrics. USG/FFRDC testing and evaluation of the software design platform developed in IDEA will be conducted throughout the course of the program, and performers are expected to address feedback from evaluations. Approval of the next funding increment will require satisfactory progress against the performer's metrics and a clear plan to achieving the program requirements and platform metrics. A program schedule with critical milestones is provided in Figure 6.

Phase 1 Milestones:

TA-1: Creation of a "no human in the loop" unified layout generator, and physical design of the benchmark circuits meeting the program metrics. Alpha, beta and public releases of the software platform and associated software modules. Complete physical design of an SoC and deliver a GDSII database ready for manufacturing at the end of Phase 1 (with the expectation of tapeout early in Phase 2).

TA-2: Development of a COTS open parts library and an intent-based system generator supporting SoCs, SiPs, and PCBs. Layout of a PCB and SiP using the TA-2 high-level synthesis tools coupled with traditional back-end physical design tools.

Phase 2 Milestones:

TA-1: Tapeout SoC in 14nm CMOS at beginning of Phase 2, and evaluate fabricated SoCs upon return. Optimize the software modules based on hardware results to feed into a 2.0 software release that is used to tapeout a second SoC. Integration of new training sets to upgrade algorithms in the final year, with a final version 3.0 release at the end of the program. The final year of the program is also expected to focus on increasing the number of users and reducing the barriers to entry for new software developers to ensure a stable, widespread user community after the program ends.

TA-2: Optimization of the first software release based on characterization of hardware fabricated at the beginning of Phase 2. Fabrication of a second round of hardware using the version 2.0 software and the IDEA layout tool, for completed automated physical design of SiPs and PCBs.

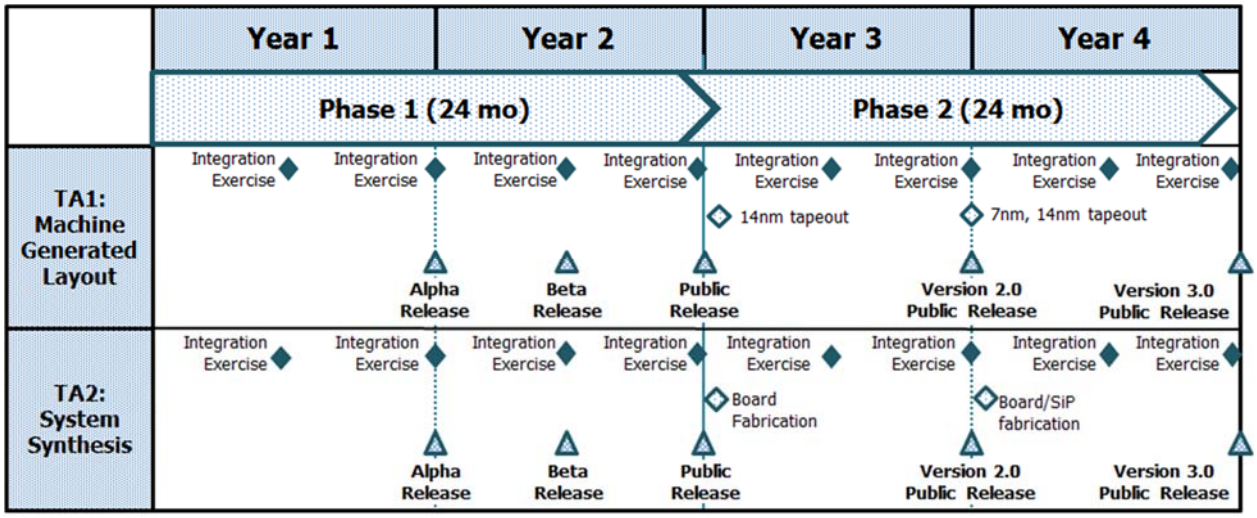

Figure 6. An illustration of the IDEA program schedule highlighting critical program events and milestones.

6. Program Deliverables

The IDEA program deliverables are summarized in Table 4.

Table 4. Summary of IDEA program deliverables by phase and technical area.

Phase	IDEA TA-1	IDEA TA-2
1	• Layout generator software and any required licenses • Trained models • Documentation • GDSII database	• System synthesis software and any required licenses • Trained Models • Documentation • Library of open COTS components

	• Reports as defined below	• Reports as defined below
2	• Layout generator software and any required licenses • Trained Models • Documentation • SoC, package and board hardware • Reports as defined below	• System synthesis software and any required licenses • Trained Models • Documentation • Library of Open COTS components • Board hardware • Reports as defined below

1. Software

Performers are required to deliver prototype (alpha), intermediate (beta) and final (public) versions of the software and accompanying documentation developed under IDEA. In Phase 1, IDEA TA-1 performers are required to release alpha, beta, and public versions of the software and deliver accompanying implementation documentation prior to the integration exercises. In Phase 2, IDEA TA-1 performers are responsible for two public software releases and are required to provide accompanying implementation documentation. For TA-2 performers, an alpha, beta and public software release is required in Phase 1, and two public software releases are required in Phase 2. TA-2 teams are expected to provide implementation documentation for each release.

2. Technical Reports

Technical reports shall be submitted as text documents on a quarterly basis beginning two weeks after the kick-off meeting. Submission of technical presentation materials will be required two working days prior to a scheduled program event, such as an integration exercise or technical interchange meeting. All reports and presentations should include a technical and management work plan that documents the project schedule including milestones. Technical interchange teleconferences to discuss software progress will be held monthly. Integration exercises, one week in length, with all performers, will be held bi-annually for the purpose of integration of software modules and demonstration of the unified physical design platforms.

3. Monthly Financial Reports

The financial report shall describe resources expended, resources available, any deviation from planned expenditures and any potential issues requiring the attention of the Government team. This report shall be provided within 10 days from the end of each month.

4. Final Report

After the end of each phase, a report shall summarize the effort in a comprehensive document.

7. Government Furnished Information

Proposers to TA-1 may expect access to a set of standard benchmarks and IP components at the beginning of Phase 1 for the purpose of evaluating the TA-1 automated physical design platform.

The benchmark suite will consist of:

- SoC benchmarks coded in Verilog RTL, with standard IP macro/primitives including cell libraries, IO buffers, and memories delivered in the LEF and LIBERTY file formats.
- Analog circuits provided as spice netlists
- SiP benchmarks provided as structured Verilog netlists
- PCB benchmarks provided as structured Verilog netlists

D. The Posh Open Source Hardware (POSH) Program

1. Program Background

POSH will bootstrap an open source SoC design and verification eco-system to enable cost effective design of ultra-complex SoCs.

Thanks to the unrelenting progress associated with Moore's Law, we now have the ability to integrate many billions of transistors on a single SoC. Unfortunately, engineering productivity has not kept pace with Moore's Law, leading to prohibitive increases in development costs and team sizes for leading edge SoCs. Currently, the main strategy for managing complexity in SoC development is through design reuse in the form of Intellectual Property (IP) modules. These IP modules are similar in nature to software library functions, and can be developed internally to an organization or procured from an external IP vendor. The current IP reuse approach has markedly improved productivity, but the single layer point-to-point approach associated with the current IP licensing model has limited the scope of reuse and abstraction.

A candidate pathway to revolutionizing SoC design is to draw from best practices in the software design community, where the advent of open source software has enabled a deep software hierarchy with many abstraction layers, significantly increasing productivity in complex system projects. Widely deployed systems, such as Android enabled smartphones and embedded devices, became practical thanks to a deeply hierarchical open source software development stack. The software abstraction model allows a software programmer to focus her/his efforts in one specific domain, while ignoring a large amount of details that would otherwise be too complex to handle. Figure 7 illustrates the key differences between modern software and hardware development.

Given the high cost of failure, adoption hurdles for open source hardware are significantly more challenging than in the software regime, necessitating development of a new set of design and validation technologies. To create a sustainable open source hardware ecosystem, the POSH program will create the technologies, methods and standards for effective open source SoC development. It is envisioned that a critical component of this effort will include development of verification technologies that provide confidence in open source hardware building blocks. POSH will also develop the supporting open source IP modules required to build high performance open source SoCs.

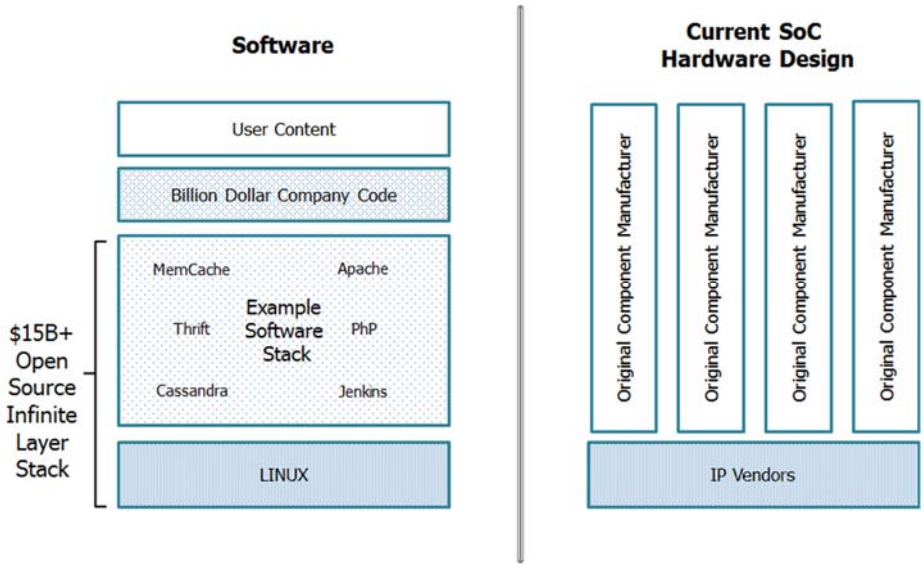

Figure 7. An illustration of the levels of abstraction in software vs hardware design.

2. Program Structure

The POSH program consists of three Technical Areas:

TA-1: Hardware Assurance Technology: Development of hardware assurance technology appropriate for signoff quality validation of deeply hierarchical analog and digital circuits of unknown origin.

TA-2: Open Source Hardware Technology: Development of design methods, standards, and critical IP components needed to kick-start a viable open source SoC eco-system.

TA-3: Open Source System-On-Chip Demonstration: Demonstration of open source hardware viability through the design of a state of the art open source System-On-Chip.

Proposals that address more than one technical area or multiple subtasks within a technical area must be constructed so that each subtask can be selected independently from one another. Proposers who include multiple subtasks in their proposal should describe each subtask separately and should provide separate pricing for each subtask.

Due to the collaborative nature of open source design, close coordination among performers in all technical areas will be critical to program success. Performers will be required to collaborate with other performers on standards, interfaces and methodologies continuously throughout the program.

Integration exercises, one week in length, will be held twice a year. All POSH performers will be required to attend and work with other performers during the integration exercise. Given the importance of open interfaces and interoperability, proposals must include a one page long Collaborative Statement that describes (1) how the proposed work will contribute to the POSH open source eco-system, (2) performer's prior experience with open collaboration, (3) a declaration of any license and copyright restrictions imposed on the delivered software and intra-

module Application Programming Interfaces (API), and (4) an affirmation, indicated by signature on the Collaborative Statement document, that the proposer accepts the requirement to collaborate with other program performers as necessary to meet the overall program goals and objectives stipulated in the BAA and the proposer's Statement of Work (SOW).

In addition to novel research, the program will emphasize delivery of working high quality software and circuits. Software and IP modules created in the program are expected to be interoperable with modules developed by other program performers, and intellectual property rights asserted by proposers are strongly encouraged to be aligned with non-viral open source licenses such as Apache 2.0, MIT, and BSD. If a proposed approach includes proprietary software or technical data as a component of the approach, the proposer is expected to provide 1) clear justification for the need for the proposed software, and 2) a description of how the POSH program goals will be met with use of the proprietary model.

3. TA-1: Hardware Assurance Technology

POSH TA-1 will develop hardware assurance technology for signoff quality validation of analog and digital circuits.

One of the reasons an open and collaborative System-On-Chip eco-system has failed to materialize is the high cost of hardware failures. A hardware bug discovered in manufactured hardware can cost commercial companies millions to billions of dollars in recalls and lost revenue. This is further magnified for the DoD, which has unique, challenging assurance and certification requirements beyond that of commercial companies. This is in contrast to the software industry, where a bug can often be fixed in the field through a low cost software update. For establishment of an open hardware eco-system, there is a need for cost effective validation technology suitable for collaborative open source development approaches.

To provide users with the confidence needed to adopt an open source component into their SoC design, POSH TA-1 takes a three-level approach to hardware assurance, as illustrated in Figure 8. Each level is considered a subtask of POSH TA-1, and proposers are encouraged to bid to one or multiple subtasks. Level 1 (L1) will provide metrics indicating IP block quality with close to zero user effort, whereas Level 2 (L2) and Level 3 (L3) will provide a high level of confidence through SoC simulation and emulation in an environment similar to the final application. The POSH TA-1 hardware assurance platform will be tested against all open source IP blocks created by performers in POSH TA-2, ensuring performance across a wide variety of circuits. It is anticipated that research breakthroughs in formal methods, parallel simulation technology, hardware emulation, and applied machine learning will be required to achieve the POSH TA-1 goals.

Critical research questions for this technical area include:

- What technologies will provide the assurance needed to make open source hardware as widely adopted as open source software?
- Can we automatically quantify assurance metrics for digital, analog, and mixed signal circuits of unknown origin?

Level	Description
L3	Accessible open API hardware emulation and prototyping platforms
L2	Scalable open API mixed accuracy simulation tools
L1	Formal tools for assessing relative and absolute quality of hardware library modules.

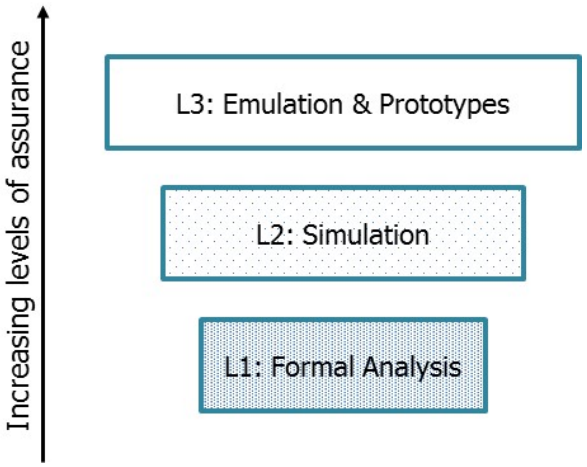

Figure 8. The above figure and associated table describes the validation platform that will be developed in POSH TA-1 and the three subtasks. Proposers may propose solutions to one or multiple subtasks.

Subtask L1: Formal Analysis

Within a vast eco-system of open source components of unknown quality, there is a need for technology that can objectively assess and effectively differentiate high quality and low quality IP blocks prior to inclusion in SoC designs. For widespread adoption, it is also critical that the assurance technology at this level requires minimal (or zero) engineering effort from the user. Formal assurance technology that enables direct analysis of the source code itself can provide an accurate estimation of quality, and help incentivize adoption of higher risk open source components.

In the commercial hardware domain, static analysis technologies exist today and are successfully applied to hardware designs, but require significant levels of user expertise. Examples of existing commercial technologies include:

- Static RTL analysis tools ("linters")
- Formal property checkers
- Code coverage analysis tools (in combination with test benches)

Proposers to POSH L1 are expected to develop formal analysis tools that go beyond existing techniques in order to provide detailed quality feedback of open source SoC modules without imposing barriers by requiring high levels of engineering effort. Performers within this subtask are expected to develop metrics ("scores") for describing and comparing the quality of open source IP designs. The POSH L1 tool is expected to support comparison of an IP block against the proposed metrics to help users rank and sort IP blocks objectively based on quality. The L1 assurance tools are expected to provide static and/or formal analysis regarding functionality, security, performance, power, and area for IP blocks that scale up to 1B transistors with zero or near zero user configuration.

Inputs to the L1 formal tools will include:

- Source code or schematics for analog and digital circuits
- Configuration and constraints

- Documentation
- Minimal testbench
- Driver software/firmware

Performers developing static assurance technology for this subtask are expected to work with performers in POSH TA-2 to define design standards and restrictions needed to facilitate the creation of the TA-1 assurance platform. Figure 9 shows a notional view of the L1 tool usage model.

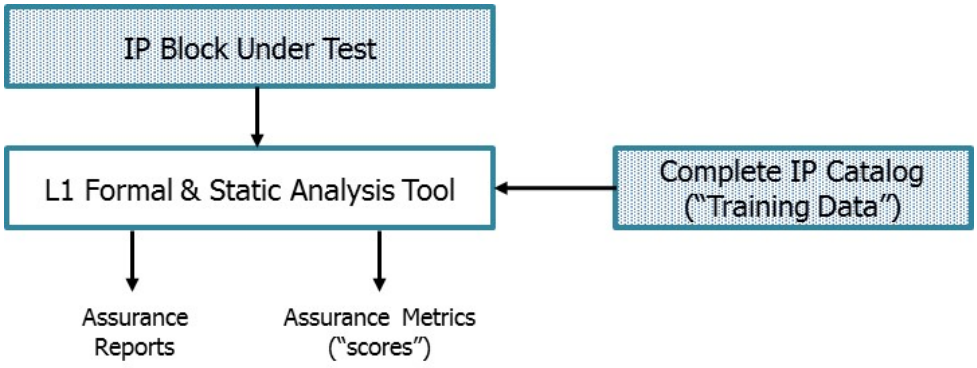

Figure 9. Notional view of the L1 subtask tool usage model.

Subtask L2: System Simulation

Today, packaged commercial software and hardware modules are delivered with extensive suites of functional unit tests and fuzzing style (random vector generator) test benches. Commercial IP module providers are incentivized to perform high quality testing due to the warranties and expectations associated with commercial terms and conditions. Unlike commercial companies, open source developers are typically not directly incentivized to create the testing and verification infrastructure needed to ensure sufficient quality, leading to drawn out community driven debugging.

While the static assurance tools developed in L1 will provide an initial quality filter for IP blocks with a minimal level of effort, functional analysis at the SoC level will be required to reach the confidence levels needed for full hardware development. Proposers to POSH subtask L2 should demonstrate a productive, fast, and cost effective simulation platform that enables application centric high assurance validation of complex SoCs.

The goal of the L2 simulation platform is to enable a high level of confidence in the quality of the open source hardware while minimizing verification efforts. A notional view of the POSH L2 simulation platform to be developed is shown in Figure 10. L2 performers will work with L3 performers to ensure that all communication APIs are compatible, enabling transparent switching between simulation and emulation. DARPA has identified the following research areas as critical to creation of the goals of subtask L2:

- Parallel cycle accurate simulation technology that scales to 1000's of servers. While simulation speed will be highly design dependent, it is anticipated that effective simulation speeds of 1 MHz can be achieved for loosely coupled digital architectures.
- Transparent and scalable co-simulation using cycle accurate simulators (e.g. https://en.wikipedia.org/wiki/Verilator) and software based processor emulation technology (e.g. http://www.qemu.org)
- Automated simulation fidelity and speed tuning at run time
- Debugging technology that enables cost effective high assurance software-only validation of highly complex SoCs designs
- Automated test case extraction for internal IP modules suitable for issue reporting to IP module authors.

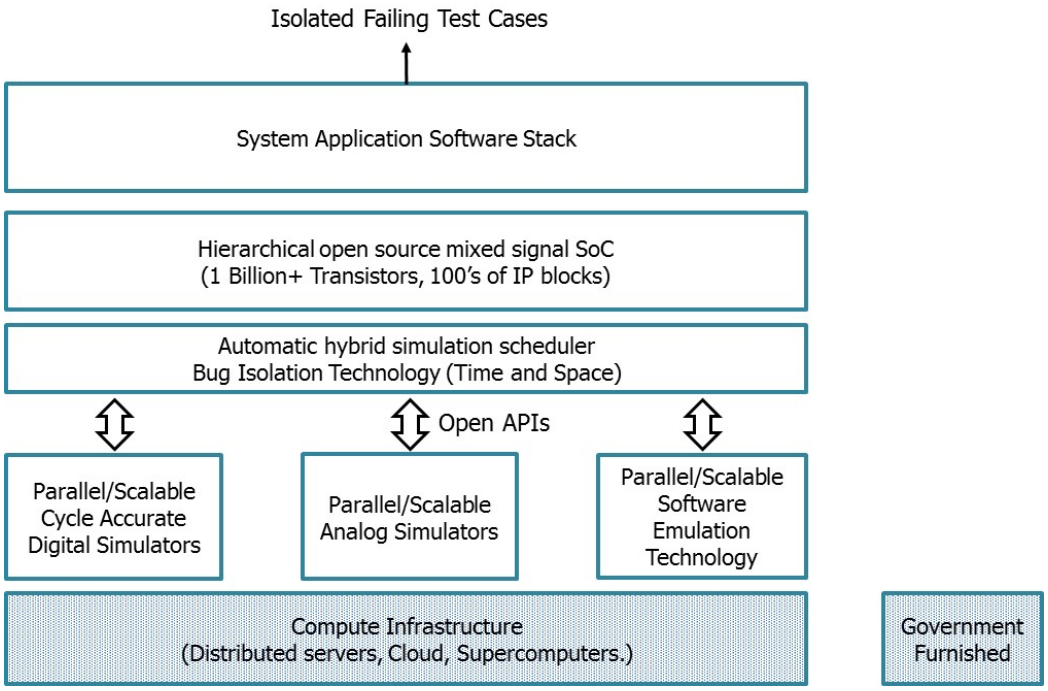

Figure 10. An illustration of the POSH TA-2 simulation platform.

Subtask L3: Hardware Emulation and Prototyping

The simulation technology developed in L2 will provide a high assurance platform for open source hardware development, but is not expected to provide sufficient assurance for commercial and DoD SoC projects that have extremely high potential field failure costs. The quality of the L2 simulation platform is inherently limited by the quality of the system models and test vectors being used, and it is likely that a number of critical bugs will be missed.

Proposers to POSH subtask L3 should demonstrate a cost effective hybrid emulation and prototyping platform to enable high assurance validation appropriate for open source SoC development.

An illustration of a notional L3 environment is shown in Figure 11. L3 performers will work with L2 performers to ensure that all communication APIs are compatible, enabling for transparent switching between simulation and emulation.

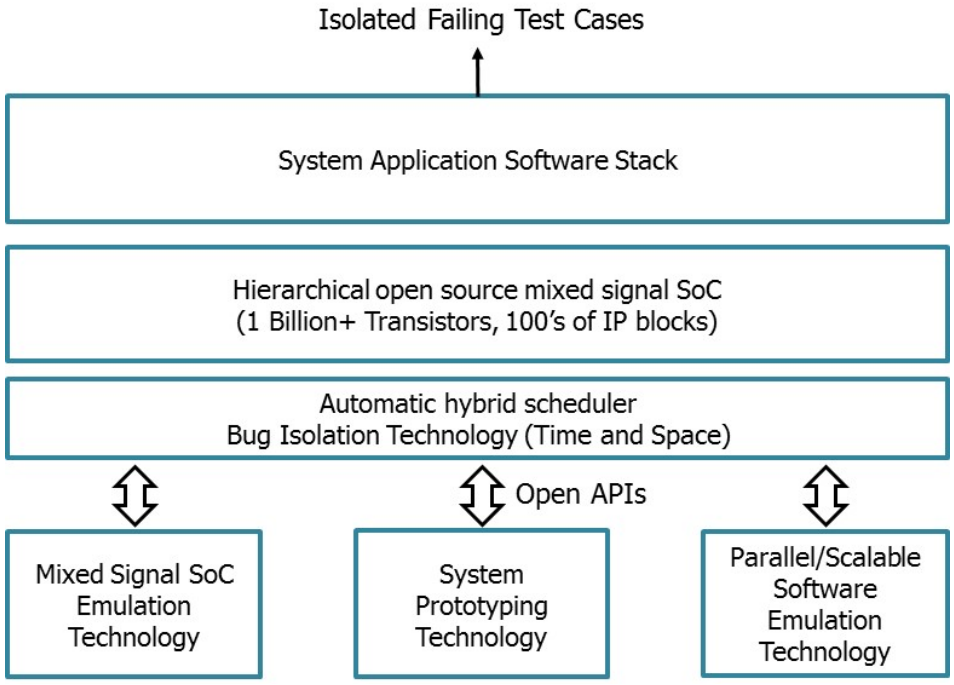

Figure 11. Illustration of the POSH L3 emulation and prototyping environment.

POSH TA-1 Goals by Phase

Phase 1: Architecture Exploration and Standards Design [Base - 24 months]

This phase will explore novel approaches in formal analysis (L1), simulation (L2), and emulation (L3) and create scalable assurance platforms commensurate with the goals of the POSH program.

During the initial 12 months of POSH TA-1, assurance platforms will be benchmarked against existing open source modules, including modules found at:

- OpenPiton (http://parallel.princeton.edu/openpiton/#infosec)
- RISC-V Rocket chip (https://github.com/freechipsproject/rocket-chip)
- Open Cores (http://opencores.org)

After 12 months, TA-1 performers will collaborate with POSH TA-2 performers to validate Alpha release open source POSH IP blocks.

At the conclusion of Phase 1, performers are expected to:

- Release design standards and communication APIs needed to meet the goals of TA-1.
- Demonstrate cost effective L1, L2, and L3 hardware assurance platforms appropriate for open source hardware development.

- Deliver software and hardware developed in TA- to demonstrate goals.

Phase 2: State-of-the-art Assurance Framework [Option – 24 months]

In Phase 2, TA-1 performers are expected to continue advancing assurance technologies developed in Phase 1 while working with POSH TA-2 and TA-3 performers to improve performance, scalability, and productivity of the platform. At the conclusion of Phase 2 performers are expected to:

- Deliver cost effective L1, L2, and L3 hardware assurance platforms with support for one billion transistor mixed signal designs, achieving:
    - Formal tools with full SoC analysis capacity
    - Simulation at 1 MHz scale speeds
    - Mixed signal emulation and prototyping of full systems
- Deliver software and hardware developed in TA-1 to demonstrate goals.

A selectable proposal for one or more subtasks of the POSH TA-1 hardware assurance platform must include the following:

- A description of the proposed solution; if proposing a solution for multiple subtasks (L1, L2, and/or L3), the proposal must be constructed so that each task can be selected independently from one another.
- A description of the unique technical merits and value provided by the technology to meet the goals of the POSH TA-1 as described above. Proposers may use prior work to argue the technical merits of their approach
- A technical description justifying how the proposed approach will exceed the state-of-the-art practices today.
- An explanation detailing how the proposed approach fits with the goal of open source collaborative SoC development.
- A description of appropriate mid-phase and end-of-phase technical metrics applicable to the evaluation of the proposed validation methodology.
- A description of the licensing model and transition path for the technology developed.
- If proposing to POSH L1, proposals should also:
    - Detail how the proposed tool will conduct analysis on open source IP modules without requiring high levels of engineering effort
    - Identify candidates for metrics that enable differentiation of open source IP block quality and include a plan for validation of the proposed metrics
    - Address how the proposed solution will provide useful feedback regarding functionality, security, performance, power, and area of IP blocks
    - Provide evidence that the approach is appropriate for open source development communities
- If proposing to POSH L2, proposals should also:
    - Discuss how simulation speeds of 1 MHz for loosely coupled systems will be achieved

  - Provide an initial plan for creation of open standard APIs for communication between the L2 and L3 tools
  - Provide technical justification for the accuracy of the proposed simulation approach
  - Provide evidence that the approach is appropriate for open source development communities
- If proposing to POSH L3, proposals should also:
  - Provide a detailed description of the proposed emulation and prototyping platform architecture
  - Discuss how the emulation and prototyping platform will support mixed signal and analog SoC circuitry
  - Provide technical justification for the accuracy of the proposed approach
  - Provide evidence that the approach is appropriate for open source development communities

4. TA-2: Open Source Hardware Design Technology

POSH TA-2 will develop a substantial collection of high quality circuits to kickstart an open source SoC eco-system.

Performers within TA-2 will develop open source SoC IP and collaborate with other TA1 and TA2 performers to formulate the basic methodologies and standards needed to ensure a thriving open source SoC design eco-system. Teams will be encouraged to share code created in this technical area on an industry-standard collaboration platform to facilitate wide adoption and ensure collaboration with TA- performers developing validation and verification methodologies. POSH TA2 will emphasize delivery of working open source circuit modules, and performers will be expected to continuously modify their code to meet the quality standards created jointly with TA-performers.

DARPA has identified an initial list of critical digital and analog SoC IP needed by a large number of SoCs, as shown in Table 5 and Table 6.

Performers may propose to develop and deliver one or multiple IP blocks; proposals addressing multiple IP blocks must be structured with separate costs per IP block. **DARPA anticipates that only one performer will be chosen per IP block.** Proposals addressing an IP block not listed in Table 5 and Table 6 must provide a thorough technical justification discussing the need for the IP block and relevance to successful creation of a complex SoC. The bulk of the effort and cost of POSH TA2 is expected to occur in Phase 1, with Phase 2 mainly targeting maintenance of the IP blocks for widespread adoption.

The expected deliverables for all IP blocks will be as follows:

For digital IP blocks:

- Source code

- User documentation
- Self-testing testbench
- Driver software/firmware

For analog IP blocks:

- ASCII based source (netlists/schematics)
- Verilog-A Model
- User documentation
- Self-testing testbench
- PDK independent support for all digital process notes from 14nm to 180nm
- Driver software/firmware

Table 5. Table listing digital circuit IP blocks that proposers may propose to develop. Proposers may develop solutions for IP blocks not listed in this table if sufficient technical justification is provided

Digital Circuit IP Blocks	Description
FPGA Fabric	https://verilogtorouting.org
A multi-core 64-bit RISC-V processor sub-system	https://riscv.org
Graphics Processing Unit (OpenGL ES 3.0)	https://www.khronos.org/opengles
PCI Express Controller	https://pcisig.com
Ethernet Controller 10/100/1G/10G/25G/40G/50G/100G	http://ethernetalliance.org
DDR Memory Controller	https://www.jedec.org/category/technology-focus-area/main-memory-ddr3-ddr4-sdram
USB 3.0 Controller	http://www.usb.org
MIPI Camera Serial Interface controller	https://www.mipi.org
CPU Subsystem	DMA, Interrupt controller, I2C, SPI, UART
H264 encoder/decoder	https://www.itu.int/rec/T-REC-H.264
AES256 encrypt/decrypt	http://nvlpubs.nist.gov/nistpubs/FIPS/NIST.FIPS.197.pdf
SHA-2/SHA-3 accelerator	https://www.nist.gov/publications/sha-3-standard-permutation-based-hash-and-extendable-output-functions?pub_id=919061
Secure Digital Controller	https://www.sdcard.org
High Definition Multimedia Interface (HDMI)	http://www.hdmi.org
Serial ATA Controller	https://www.sata-io.org

JESD204B Controller	https://www.jedec.org/sites/default/files/docs/JESD204B.pdf
NAND Flash Controller	http://www.onfi.org
CAN Controller	https://www.iso.org/standard/63648.html

Table 6. Table listing analog/mixed signal circuit IP blocks that proposers may propose to develop. Proposers may develop solutions for IP blocks not listed in this table if sufficient technical justification is provided.

Analog/Mixed Signal Circuit IP Blocks	Description
Standard I/O interfaces PHYs	DDR, PCIe, SATA, USB, XAUI, CPRI
PLL	Range: 10MHz – 10GHz (multiple circuits or generators)
DLL	Range: 10Mhz – 10GHz (multiple circuits or generators)
Analog to Digital Converters	Range: 1 – 10,000 MSPS (multiple circuits or generators)
Digital to Analog Converters	Range: 1 – 10,000 MSPS (multiple circuits or generators)
Voltage Regulators	Input: 1.8V – 12V, Output 0.25V – 1.8V (multiple circuits)
Monitor circuits	Temperature, voltage, process

Phase 1: Subsystem Creation [Base – 24 months]
In Phase 1, TA2 performers are expected to develop and deliver PDK independent analog and digital open source IP modules and work with POSH TA-1 teams to verify and adapt their code as needed. This includes:

1. Demonstration of cost efficient open source design of mixed signal/analog circuits.
2. Demonstration of complete decoupling of design sources and PDK data.
3. Demonstration of portability from 14nm to 180nm technology nodes.
4. Delivery of all circuit source code, testbenches, models, and requisite documentation.

Phase 2: Open Source Subsystem Maintenance [Option – 24 months]
In Option Phase 2 of POSH TA2, performers will provide maintenance support and improvements for the open source IP blocks created in Phase 1 and expand the user community. Performers will be expected to collaborate with POSH TA-1 performers and modify the IP blocks as necessary to create a higher quality IP block.

A selectable proposal must include the following, where applicable:

- A description of the IP design approach and how it is well suited for open source SoC collaborative design.
- Evidence of cost effective open source circuit development.
- A description of each proposed IP block solution, costed separately.
- A description of appropriate mid-phase and end-of-phase technical metrics applicable to the evaluation of the proposed IP block.
- A description of how IP delivery methods and design methodologies will be standardized
- A description of the proposer's anticipated open source circuit release schedule

- Public releases of circuit sources are required at the end of each phase
- At a minimum, controlled releases should occur on an industry-leading open source platform at 12 months in Phase 1. Additional releases to facilitate integration are strongly encouraged

5. TA-3: Open Source System-on-Chip Demonstration:

POSH TA3 will develop a high performing open source 14nm CMOS System-On-Chip using technologies from TA-1 and TA2.

A limited number of highly innovative proposals will be considered for creation of high performance SoCs that demonstrate the effectiveness of the open source ecosystem supported by POSH TA1 and TA-2. TA-3 performers will be expected to participate in and drive standards development for POSH TA-2 performers and create SoC hardware architectures that integrate a large portion of the analog and digital open source IP library components released in TA-2. DARPA envisions research in this technical area will include exploration of new hardware architectures enabled by the POSH open source hardware ecosystem and will demonstrate the performance benefits of increasing levels of abstraction.

Teams will be expected to conduct system architecture studies and create additional application specific components to be integrated in the open source SoC in addition to using POSH IP components developed in TA-2. The proposal must identify the relevant use cases of the proposed SoC, address the relevance of the proposed research to the objectives of the POSH program and National Security, and provide technical justification describing how the proposed SoC will advance the state of the art.

The proposed SoC is expected to target the 14/16nm CMOS technology node with a maximum size of 10x10mm. DARPA will provide fabrication support for proposers to POSH TA-3 through a number of separately funded multi-project or dedicated wafer runs; therefore, fabrication costs should not be included in proposal budgets.

Phase 1: SoC Design and Verification [Base - 24 months]
In Phase 1 of POSH TA-3 performers are expected to collaborate with POSH TA-1 and TA-2 performers to complete initial design, verification, and pre-tapeout prototyping of the SoC in preparation for a Phase 2 Option tapeout:

- In the initial 12 months of Phase 1, work collaboratively with POSH TA-2 performers to define standards for open source digital and analog IP.
- Complete exploration of the system architecture and design of specialized components required in addition to POSH TA-2 IP. The SoC is expected to integrate the majority of standard IP blocks from TA-2 performers, as listed in Table 5 and Table 6.
- Validate the complete SoC design using hardware assurance technologies from POSH TA-1.
- Deliver complete source code and documentation of the proposed SoC.

- Complete physical design of the SoC and produce a deliver a GDSII database ready for manufacturing at the end of Phase 1.

Phase 2: System Validation [Option – 24 months]
In Phase 2 of POSH TA-3, performers will continue advancing the SoC developed in Phase 1 and demonstrate an operational high performance open source SoC:

- A tapeout at the 14/16nm technology node is expected to occur early in Phase 2. After fabrication, teams will verify the SoC through characterization and demonstration of all functionality and peripherals
- Results from the first tapeout should be used to optimize and redesign the SoC in preparation for a second tapeout that will demonstrate a SoC with higher performance.
- Deliver complete source code and documentation of the proposed 2nd generation SoC
- Complete physical design of the SoC and produce a deliver a GDSII database ready for manufacturing at the end of Phase 2.

A selectable proposal for POSH TA-3 must include the following:

- Evidence that the SWaP-C metrics of the proposed SoC exceed existing COTS based solutions by 10x.
- A description describing how the proposed SoC helps achieve the stated POSH program goal of "bootstrap an open source SoC design and verification eco-system to enable cost effective design of ultra-complex SoCs."
- A description of the unique technical merits and value provided by the technology to national security. Proposers may use prior work to argue the technical merits of their approach.
- A description of the approach used to manage integration and verification complexity of the full SoC development.

6. Schedule and Milestones

The POSH program schedule consists of a 24-month base period (Phase 1), followed by a 24-month option period (Phase 2), for a total of 48 months, subject to availability of funds and technical progress achieved. Due to the likelihood that performers will be developing building blocks and contributions to the hardware assurance platform, proposers will be required to establish intermediate goals and milestones that support their strategies.

All performers will be assessed throughout the program based on their individual technical progress as well as through evaluations conducted by USG/FFRDC. Approval of the next funding increment will require satisfactory progress against the performer's metrics and a clear plan to achieving the program requirements. A program schedule with critical milestones is provided in Figure 12.

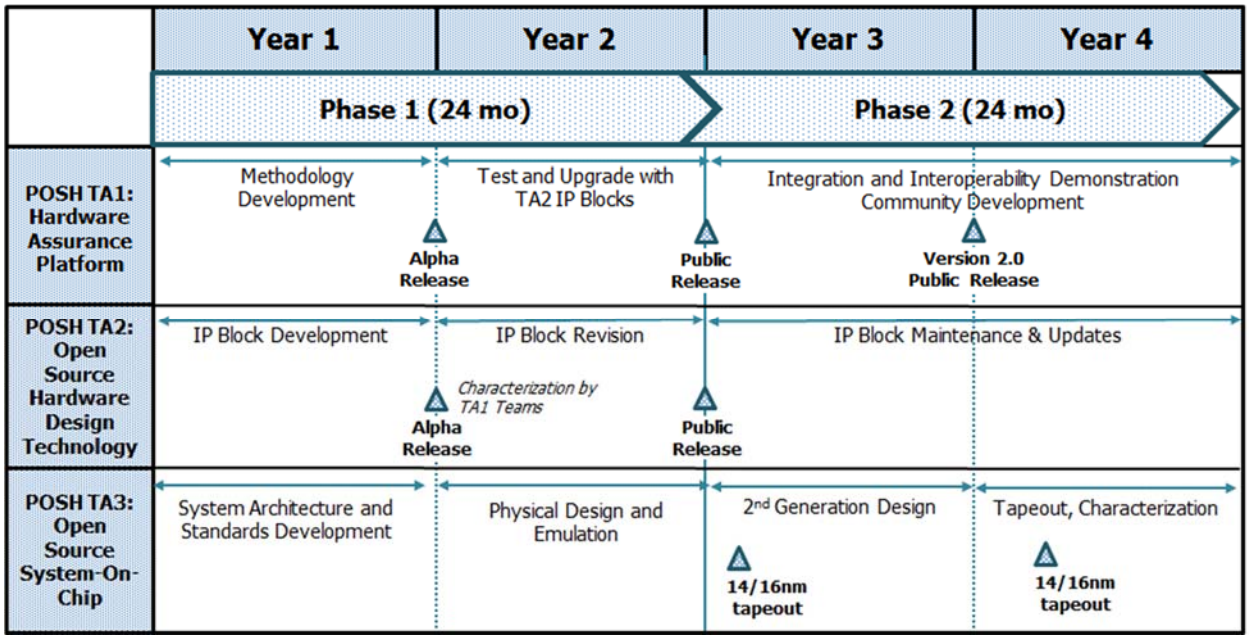

Figure 12. An Illustration of the POSH program schedule highlighting critical program events and milestones.

7. Program Deliverables

The POSH program deliverables are summarized in Table 7. A written description of each deliverable can be found below the table.

Table 7. A summary of POSH program deliverables by phase and technical area

Phase	POSH TA-1	POSH TA-2	POSH TA-3
1	• Software and any required licenses • Training Models • Documentation • Reports as defined below	• IP Blocks • Supporting documentation • Reports as defined below	• Specialized IP blocks • GDSII database ready for manufacturing • Reports as defined below
2	• Software and any required licenses • Training Models • Documentation • Reports as defined below	• IP Blocks • Supporting documentation • Reports as defined below	• SoC, package and board (hardware) • Reports as defined below

1. Software

TA-1 performers are required to deliver the software developed in POSH along with appropriate documentation.

2. Performer developed open source IP Blocks

TA-2 performers are required to deliver design data for all developed IP, including documentation, schematics/sources, design models, and test benches as appropriate.

3. Technical Reports

Technical reports shall be submitted as text documents on a quarterly basis beginning two weeks after the kick-off meeting. Submission of technical presentation materials will be required two working days prior to a scheduled program event, such as an integration exercise or technical interchange meeting. All reports and presentations should include a technical and management work plan that documents the project schedule including milestones. One-week long integration exercises with all performers will be held bi-annually and will be tied to integration of the hardware assurance platform and evaluation of open source IP blocks.

4. Monthly Financial Reports

The financial report shall describe resources expended, resources available, any deviation from planned expenditures and any potential issues requiring the attention of the Government team. This report shall be provided within 10 days from the end of each month.

5. Final Report

After the end of each phase, a report shall summarize the effort in a comprehensive document.

II. Award Information

A. General Award Information

Multiple awards are anticipated. The amount of resources made available under this BAA will depend on the quality of the proposals received and the availability of funds.

The Government reserves the right to select for negotiation all, some, one, or none of the proposals received in response to this solicitation, and to make awards without discussions with proposers. The Government also reserves the right to conduct discussions if it is later determined to be necessary. If warranted, portions of resulting awards may be segregated into pre-priced options. Additionally, DARPA reserves the right to accept proposals in their entirety or to select only portions of proposals for award. In the event that DARPA desires to award only portions of a proposal, negotiations may be opened with that proposer. The Government reserves the right to fund proposals in phases with options for continued work at the end of one or more of the phases, as applicable.

Awards under this BAA will be made to proposers on the basis of the evaluation criteria listed below (see section labeled “Application Review Information,” Sec. V.), and program balance to provide overall value to the Government. The Government reserves the right to request any additional, necessary documentation once it makes the award instrument determination. Such additional information may include but is not limited to Representations and Certifications (see Section VI.B.4., “Representations and Certifications”). The Government reserves the right to remove proposers from award consideration should the parties fail to reach agreement on award terms, conditions and cost/price within a reasonable time or the proposer fails to timely provide

requested additional information. Proposals identified for negotiation may result in a procurement contract, grant, cooperative agreement, or other transaction, depending upon the nature of the work proposed, the required degree of interaction between parties, whether or not the research is classified as Fundamental Research, and other factors.

Proposers looking for innovative, commercial-like contractual arrangements are encouraged to consider requesting Other Transactions. To understand the flexibility and options associated with Other Transactions, consult http://www.darpa.mil/work-with-us/contract-management#OtherTransactions. In addition, an "ERI Page 3 Investments" Technology Investment Agreement (TIA) "Model", and companion document, are available for review at http://darpa.mil/work-with-us/electronics-resurgence-initiative. Any questions pertaining to the use of Other Transactions should be directed to the BAA email address provided herein.

In all cases, the Government contracting officer shall have sole discretion to select award instrument type, regardless of instrument type proposed, and to negotiate all instrument terms and conditions with selectees. DARPA will apply publication or other restrictions, as necessary, if it determines that the research resulting from the proposed effort will present a high likelihood of disclosing performance characteristics of military systems or manufacturing technologies that are unique and critical to defense. Any award resulting from such a determination will include a requirement for DARPA permission before publishing any information or results on the program. For more information on publication restrictions, see the section below on Fundamental Research.

B. Fundamental Research

It is DoD policy that the publication of products of fundamental research will remain unrestricted to the maximum extent possible. National Security Decision Directive (NSDD) 189 defines fundamental research as follows:

> 'Fundamental research' means basic and applied research in science and engineering, the results of which ordinarily are published and shared broadly within the scientific community, as distinguished from proprietary research and from industrial development, design, production, and product utilization, the results of which ordinarily are restricted for proprietary or national security reasons.

As of the date of publication of this BAA, the Government expects that program goals as described herein may be met by proposers intending to perform fundamental research and proposers not intending to perform fundamental research or the proposed research may present a high likelihood of disclosing performance characteristics of military systems or manufacturing technologies that are unique and critical to defense. Based on the nature of the performer and the nature of the work, the Government anticipates that some awards will include restrictions on the resultant research that will require the awardee to seek DARPA permission before publishing any information or results relative to the program.

Proposers should indicate in their proposal whether they believe the scope of the research included in their proposal is fundamental or not. While proposers should clearly explain the intended results of their research, the Government shall have sole discretion to select award

instrument type and to negotiate all instrument terms and conditions with selectees. Appropriate clauses will be included in resultant awards for non-fundamental research to prescribe publication requirements and other restrictions, as appropriate. This clause can be found at http://www.darpa.mil/work-with-us/additional-baa.

For certain research projects, it may be possible that although the research being performed by the awardee is restricted research, a subawardee may be conducting fundamental research. In those cases, it is the awardee's responsibility to explain in their proposal why its subawardee's effort is fundamental research

III. Eligibility Information

A. Eligible Applicants

All responsible sources capable of satisfying the Government's needs may submit a proposal that shall be considered by DARPA.

1. Federally Funded Research and Development Centers (FFRDCs) and Government Entities

a) FFRDCs

FFRDCs are subject to applicable direct competition limitations and cannot propose to this BAA in any capacity unless they meet the following conditions: (1) FFRDCs must clearly demonstrate that the proposed work is not otherwise available from the private sector. (2) FFRDCs must provide a letter on official letterhead from their sponsoring organization citing the specific authority establishing their eligibility to propose to Government solicitations and compete with industry, and their compliance with the associated FFRDC sponsor agreement's terms and conditions. This information is required for FFRDCs proposing to be awardees or subawardees.

b) Government Entities

Government Entities (e.g., Government/National laboratories, military educational institutions, etc.) are subject to applicable direct competition limitations. Government entities must clearly demonstrate that the work is not otherwise available from the private sector and provide written documentation citing the specific statutory authority and contractual authority, if relevant, establishing their ability to propose to Government solicitations.

c) Authority and Eligibility

At the present time, DARPA does not consider 15 U.S.C. § 3710a to be sufficient legal authority to show eligibility. While 10 U.S.C.§ 2539b may be the appropriate statutory starting point for some entities, specific supporting regulatory guidance, together with evidence of agency approval, will still be required to fully establish eligibility. DARPA will consider FFRDC and

Government entity eligibility submissions on a case-by-case basis; however, the burden to prove eligibility for all team members rests solely with the proposer.

2. Non-U.S. Organizations and/or Individuals

Non-U.S. organizations and/or individuals may participate to the extent that such participants comply with any necessary nondisclosure agreements, security regulations, export control laws, and other governing statutes applicable under the circumstances.

B. Organizational Conflicts of Interest

FAR 9.5 Requirements

In accordance with FAR 9.5, proposers are required to identify and disclose all facts relevant to potential OCIs involving the proposer's organization and *any* proposed team member (subawardee, consultant). Under this Section, the proposer is responsible for providing this disclosure with each proposal submitted to the BAA. The disclosure must include the proposer's, and as applicable, proposed team member's OCI mitigation plan. The OCI mitigation plan must include a description of the actions the proposer has taken, or intends to take, to prevent the existence of conflicting roles that might bias the proposer's judgment and to prevent the proposer from having unfair competitive advantage. The OCI mitigation plan will specifically discuss the disclosed OCI in the context of each of the OCI limitations outlined in FAR 9.505-1 through FAR 9.505-4.

Agency Supplemental OCI Policy

In addition, DARPA has a supplemental OCI policy that prohibits contractors/performers from concurrently providing Scientific Engineering Technical Assistance (SETA), Advisory and Assistance Services (A&AS) or similar support services and being a technical performer. Therefore, as part of the FAR 9.5 disclosure requirement above, a proposer must affirm whether the proposer or *any* proposed team member (subawardee, consultant) is providing SETA, A&AS, or similar support to any DARPA office(s) under: (a) a current award or subaward; or (b) a past award or subaward that ended within one calendar year prior to the proposal's submission date.

If SETA, A&AS, or similar support is being or was provided to any DARPA office(s), the proposal must include:

- The name of the DARPA office receiving the support;
- The prime contract number;
- Identification of proposed team member (subawardee, consultant) providing the support; and
- An OCI mitigation plan in accordance with FAR 9.5.

Government Procedures

In accordance with FAR 9.503, 9.504 and 9.506, the Government will evaluate OCI mitigation plans to avoid, neutralize or mitigate potential OCI issues before award and to determine whether it is in the Government's interest to grant a waiver. The Government will only evaluate OCI mitigation plans for proposals that are determined selectable under the BAA evaluation criteria and funding availability.

The Government may require proposers to provide additional information to assist the Government in evaluating the proposer's OCI mitigation plan.

If the Government determines that a proposer failed to fully disclose an OCI; or failed to provide the affirmation of DARPA support as described above; or failed to reasonably provide additional information requested by the Government to assist in evaluating the proposer's OCI mitigation plan, the Government may reject the proposal and withdraw it from consideration for award.

C. Cost Sharing/Matching

Cost sharing is not required; however, it will be carefully considered where there is an applicable statutory condition relating to the selected funding instrument. Cost sharing is encouraged where there is a reasonable probability of a potential commercial application related to the proposed research and development effort.

For more information on potential cost sharing requirements for Other Transactions, see http://www.darpa.mil/work-with-us/contract-management#OtherTransactions.

D. Other Eligibility Criteria

1. Collaborative Efforts

Collaborative efforts/teaming are encouraged. After proposal selections, the Government reserves the right to seek contractual arrangements, such as Associate Contractor Agreements (ACAs), between separate performers if doing so benefits the overall program/project goals and objectives and mutual interests of the parties.

IV. Application and Submission Information

PROPOSERS ARE CAUTIONED THAT EVALUATION RATINGS MAY BE LOWERED AND/OR PROPOSALS REJECTED IF PROPOSAL PREPARATION (PROPOSAL FORMAT, CONTENT, ETC.) AND/OR SUBMITTAL INSTRUCTIONS ARE NOT FOLLOWED.

A. Address to Request Application Package

This announcement, any attachments, and any references to external websites herein constitute the total solicitation. If proposers cannot access the referenced material posted in the announcement found at www.darpa.mil, contact the administrative contact listed herein.

B. Content and Form of Application Submission

1. Full Proposal Format

All full proposals must be in the format given below. Proposals shall consist of two volumes: Volume I – Technical and Management Proposal (3 sections), and Volume II – Cost Proposal (4

sections). All pages shall be printed on 8-1/2 by 11 inch paper with type not smaller than 12 point. Smaller font may be used for figures, tables and charts. The page limitation for full proposals includes all figures, tables, and charts. The submission of other supporting materials along with the proposals is strongly discouraged and will not be considered for review. Section II of Volume I, Technical and Management Proposal, shall not exceed 20 pages. There is no page limit for Volume II, Cost Proposal. All full proposals must be written in English.

A summary slide of the proposed effort, in PowerPoint format, should be submitted with the proposal. A template slide is provided as Attachment 2 to the BAA. Submit this PowerPoint file in addition to Volumes I and II of your full proposal. This summary slide does not count towards the total page count.

When proposing to multiple programs, proposers are required to propose solutions for IDEA and/or POSH in separate proposals. **Proposers should not propose to more than one program in a single proposal.** Proposals that address more than one technical area or multiple subtasks within a technical area must be constructed so that each subtask can be selected independently from one another. Proposers who include multiple subtasks in their proposal should describe each subtask separately and should provide separate costing for each subtask.

a. Volume I, Technical and Management Proposal

Section I. Administrative

A. Cover sheet to include:

(1) BAA number (HR001117S0054);
(2) Program Name and Technical area(s)/Sub-task(s);
(3) Lead Organization submitting proposal;
(4) Type of organization, selected among the following categories:
Large Organization, Small Disadvantaged Organization, Other Small Organization, HBCU, MI, Other Educational, Other Nonprofit;
(5) Proposer's internal reference number (if any);
(6) Other team members (if applicable) and type of organization for each;
(7) Proposal title;
(8) Technical point of contact to include:
Salutation, last name, first name, street address, city, state, zip code (+4), telephone, fax (if available), electronic mail;
(9) Administrative point of contact to include:
Salutation, last name, first name, street address, city, state, zip code (+4), telephone, fax (if available), electronic mail;
(10) Total funds requested from DARPA, and the amount of cost share (if any); AND
(11) Date proposal was submitted.

B. Official transmittal letter.

The transmittal letter should identify the BAA number with specific program listed, the proposal by name, and the proposal reference number (if any), and should be signed by an individual who is authorized to submit proposals to the Government.

Section II. Detailed Proposal Information

A. Statement of Work (SOW)

In plain English, clearly define the technical tasks/subtasks to be performed, their durations, and dependencies among them. The page length for the SOW will be dependent on the amount of the effort. For each task/subtask, provide:

1. A general description of the objective (for each defined task/activity);
2. A detailed description of the approach to be taken to accomplish each defined task/activity;
3. Identification of the primary organization responsible for task execution (prime, sub, team member, by name, etc.);
4. The completion criteria for each task/activity - a product, event or milestone that defines its completion.
5. Define all deliverables (reporting, data, reports, software, etc.) to be provided to the Government in support of the proposed research tasks/activities; AND
6. Clearly identify any tasks/subtasks (prime or subcontracted) that will be accomplished on-campus at a university, if applicable..

Note: Each Technical Area, Phase, and subtask, as applicable, of the program must be separately defined in the SOW. Include a SOW for each subcontractor and/or consultant in the ***Cost Proposal Volume****. Do not include any proprietary information in the SOW(s).*

B. Collaborative Statement

Given the importance of open interfaces and interoperability between software modules, proposals should include a one page long Collaborative Statement that describes

1. How the proposed work will be integrated within the program design flow
2. Performer's prior experience with open collaboration
3. A declaration of any license and copyright restrictions imposed on the delivered software and intra-module Application Programming Interfaces (API).
4. An affirmation, indicated by signature on the Collaborative Statement document, that the proposer accepts the requirement to collaborate with other program performers as necessary to meet the overall program goals and objectives stipulated in the BAA and the proposer's Statement of Work (SOW).

C. Results and Technology Transfer

Successful transition is incredibly important under the Electronics Resurgence Initiative, which was created with an emphasis on impact. Proposals with an expected outcome limited to scientific papers, new ideas, or patents acquired without tangible, product-based impact on national defense will not be strongly considered. It is critical to design a transition plan for further maturing the technology and moving it from the developer to commercial and DoD users.

Proposers should describe their initial hypothesis on how this technology will transition from lab to market and DoD impact. Describe what would be sold, who would make it, who would

buy it, and what impact it would have. Proposals should include a costed task associated with building a viable transition plan.

D. Technical Approach

This section is the centerpieces of the proposal and should succinctly summarize the innovative claims for the proposed research and clearly describe the proposed approach without using any jargon. This section should demonstrate that the proposer has a clear understanding of the state-of-the-art and should provide sufficient justification for the feasibility of the proposed approach(es). This section should include a detailed technical rationale, technical approach, and constructive plan for accomplishment of technical goals in support of innovative claims and deliverable creation.

Proposers should use the items and questions listed in Section C for IDEA and Section D for POSH as reference in building their technical approach.

E. Ongoing Research

Thoroughly and quantitatively describe the uniqueness and benefits of the proposed approach relative to the current state-of-art and alternate approaches. This section should include a comparison of the proposed effort with ongoing research, indicating the advantages and disadvantages of the proposed approach.

F. Risk Analysis and Mitigation Plan

Identify the major technical and programmatic risks in the program. Include a risk matrix. For each risk, assign a probability of occurrence on a scale of 1-10, where 10 indicates a high likelihood that the risk will impact program success, as well as an assessment of impact, also on a scale of 1-10, where 10 indicates that this risk would maximally limit the program from delivering software on schedule or meeting performance objectives. For each item with total risk (likelihood × impact) exceeding 40, include a plan for mitigating the risk and assessing risk reduction.

G. Proposer Accomplishments

This section should include a discussion of proposer's previous accomplishments and work in closely related research areas.

H. Teaming

Describe the formal teaming arrangements that will be used to execute this effort. Describe the programmatic relationship between investigators and the rationale for choosing this teaming strategy. Present a coherent organization chart and integrated management strategy for the program team. For each person, indicate: (1) name, (2) affiliation, (3) abbreviated listing of all technical area tasks they will work on with roles, responsibilities, and percent time indicated, (4) discussion of the proposers' previous accomplishments, relevant expertise and/or unique capabilities.

I. Schedules and measurable milestones
Schedules and measurable milestones for the proposed research. (Note: Measurable milestones should capture key development points in tasks and should be clearly articulated and defined in time relative to start of effort.) Where the effort consists of multiple portions which could reasonably be partitioned for purposes of funding, these should be identified as options. Additionally, proposals should clearly explain the technical approach(es) that will be employed to meet or exceed each program metric and provide ample justification as to why the approach(es) is/are feasible. The milestones must not include proprietary information.

Section III. Additional Information

Information in this section may include an attached bibliography of relevant technical papers or research notes (published and unpublished) which document the technical ideas and approach upon which the proposal is based. Copies of not more than three (3) prior relevant papers may be included with the submission. The bibliography and attached papers are not included in the page counts given.

b. Volume II, Cost Proposal – {No Page Limit}

All proposers, including FFRDCs, must submit the following:

Section I. Administrative

Cover sheet to include:
(1) BAA number (HR001117S0054);
(2) Program Name and Technical area(s)/Sub-tasks;
(3) Lead Organization submitting proposal;
(4) Type of organization, selected among the following categories:
Large Organization, Small Disadvantaged Organization, Other Small Organization, HBCU, MI, Other Educational, Other Nonprofit;
(5) Proposer's internal reference number (if any);
(6) Other team members (if applicable) and type of organization for each;
(7) Proposal title;
(8) Technical point of contact to include:
Salutation, last name, first name, street address, city, state, zip code (+4), telephone, fax (if available), electronic mail (if available);
(9) Administrative point of contact to include:
Salutation, last name, first name, street address, city, state, zip code (+4), telephone, fax (if available), and electronic mail (if available);
(10) Award instrument requested:
Cost-Plus-Fixed Fee (CPFF), Cost-contract—no fee, cost sharing contract—no fee, or other type of procurement contract (*specify*), Grant, Cooperative Agreement, or Other Transaction;
(11) Place(s) and period(s) of performance;
(12) Total proposed cost separated by basic award and option(s), if any, by calendar year and by government fiscal year;

(13) Name, address, and telephone number of the proposer's cognizant Defense Contract Management Agency (DCMA) administration office (*if known)*;
(14) Name, address, and telephone number of the proposer's cognizant Defense Contract Audit Agency (DCAA) audit office (*if known*);
(15) Date proposal was prepared;
(16) DUNS number;
(17) TIN number;
(18) CAGE Code;
(19) Subcontractor Information;
(20) Proposal validity period (120 days is recommended); AND
(21) Any Forward Pricing Rate Agreement, other such approved rate information, or such documentation that may assist in expediting negotiations (if available).

Attachment 1, the Cost Volume Proposer Checklist, must be included with the coversheet of the Cost Proposal.

Section II. Detailed Cost Information (Prime and Subcontractors)

The proposers', to include eligible FFRDCs', cost volume shall provide cost and pricing information (See Note 1), or other than cost or pricing information if the total price is under the referenced threshold, in sufficient detail to substantiate the program price proposed (e.g., realism and reasonableness). In doing so, the proposer shall provide, **for both the prime and each subcontractor**, a "Summary Cost Breakdown" by phase and performer fiscal year, and a "Detailed Cost Breakdown" by phase, technical task/sub-task, and month. The breakdown/s shall include, at a minimum, the following major cost items along with associated backup documentation:

Total program cost broken down by major cost items:

A. Direct Labor
A breakout clearly identifying the individual labor categories with associated labor hours and direct labor rates, as well as a detailed Basis-of-Estimate (BOE) narrative description of the methods used to estimate labor costs;

B. Indirect Costs
Including Fringe Benefits, Overhead, General and Administrative Expense, Cost of Money, Fee, etc. (must show base amount and rate);

C. Travel
Provide the purpose of the trip, number of trips, number of days per trip, departure and arrival destinations, number of people, etc.;

D. Other Direct Costs
Itemized with costs; back-up documentation is to be submitted to support proposed costs;

E. Material/Equipment

(i) For IT and equipment purchases, include a letter stating why the proposer cannot provide the requested resources from its own funding.
(ii) A priced Bill-of-Material (BOM) clearly identifying, for each item proposed, the quantity, unit price, the source of the unit price (i.e., vendor quote, engineering estimate, etc.), the type of property (i.e., material, equipment, special test equipment, information technology, etc.), and a cross-reference to the Statement of Work (SOW) task/s that require the item/s. At time of proposal submission, any item that exceeds $1,000 must be supported with basis-of-estimate (BOE) documentation such as a copy of catalog price lists, vendor quotes or a written engineering estimate (additional documentation may be required during negotiations, if selected).
(iii) If seeking a procurement contract and items of Contractor Acquired Property are proposed, exclusive of material, the proposer shall clearly demonstrate that the inclusion of such items as Government Property is in keeping with the requirements of FAR Part 45.102. In accordance with FAR 35.014, "Government property and title," it is the Government's intent that title to all equipment purchased with funds available for research under any resulting contract will vest in the acquiring nonprofit institution (e.g., Nonprofit Institutions of Higher Education and Nonprofit Organizations whose primary purpose is the conduct of scientific research) upon acquisition without further obligation to the Government. Any such equipment shall be used for the conduct of basic and applied scientific research. The above transfer of title to all equipment purchased with funds available for research under any resulting contract is not allowable when the acquiring entity is a for-profit organization; however, such organizations can, in accordance with FAR 52.245-1(j), be given priority to acquire such property at its full acquisition cost.

F. Consultants

If consultants are to be used, proposer must provide a copy of the consultant's proposed SOW as well as a signed consultant agreement or other document which verifies the proposed loaded daily / hourly rate and any other proposed consultant costs (e.g. travel);

G. Subcontracts

Itemization of all subcontracts. Additionally, the prime contractor is responsible for compiling and providing, as part of its proposal submission to the Government, subcontractor proposals prepared at the same level of detail as that required by the prime. Subcontractor proposals include Interdivisional Work Transfer Agreements (ITWA) or similar arrangements. If seeking a procurement contract, the prime contractor shall provide a cost reasonableness analysis of all proposed subcontractor costs/prices. Such analysis shall indicate the extent to which the prime contractor has negotiated subcontract costs/prices and whether any such subcontracts are to be placed on a sole-source basis.

All proprietary subcontractor proposal documentation, prepared at the same level of detail as that required of the prime, which cannot be uploaded to the DARPA BAA website (https://baa.darpa.mil, BAAT) or Grants.gov as part of the proposer's submission, shall be made immediately available to the Government, upon request, under separate cover (i.e., mail, electronic/email, etc.), either by the proposer or by the subcontractor organization. This does not relieve the proposer from the requirement to include, as part of their submission (via

BAAT or Grants.gov, as applicable), subcontract proposals that do not include proprietary pricing information (rates, factors, etc.).

A Rough Order of Magnitude (ROM), or similar budgetary estimate, is not considered a fully qualified subcontract cost proposal submission. Inclusion of a ROM, or similar budgetary estimate, may result in the full proposal being deemed non-compliant or evaluation ratings may be lowered;

H. Cost-Sharing

The amount of any industry cost-sharing (the source and nature of any proposed cost-sharing should be discussed in the narrative portion of the cost volume); AND

I. Fundamental Research

Written justification required per Section II.B, "Fundamental Research," pertaining to prime and/or subcontracted effort being considered Contracted Fundamental Research.

Note 1:
(a) "Cost or Pricing Data" as defined in FAR 15.403-4 shall be required if the proposer is seeking a procurement contract per the referenced threshold, unless the proposer requests and is granted an exception from the requirement to submit cost or pricing data. Per DFARS 215.408(5), DFARS 252.215-7009, Proposal Adequacy Checklist, applies to all proposers/proposals seeking a FAR-based award (contract).
(b) In accordance with DFARS 15.403-1(4)(D), DoD has waived cost or pricing data requirements for nonprofit organizations (including educational institutions) on cost-reimbursement-no-fee contracts. In such instances where the waiver stipulated at DFARs 15.403-1(4)(D) applies, proposers shall submit information other than cost or pricing data to the extent necessary for the Government to determine price reasonableness and cost realism; and cost or pricing data from subcontractors that are not nonprofit organizations when the subcontractor's proposal exceeds the cost and pricing data threshold at FAR 15.403-4(a)(1).
(c) Per Section 873 of the FY2016 National Defense Authorization Act (Pub L. 114-92), "Pilot Program For Streamlining Awards For Innovative Technology Projects," small businesses and nontraditional defense contractors (as defined therein) are alleviated from submission of certified cost and pricing data for new contract awards valued at less than $7,500,000. In such instances where this "waiver" applies, proposers seeking a FAR-based contract shall submit information other than certified cost or pricing data to the extent necessary for the Government to determine price reasonableness and cost realism; and certified cost or pricing data from subcontractors that are not small businesses or nontraditional defense contractors when such subcontract proposals exceed the cost and pricing data threshold at FAR 15.403-4(a)(1).
(d) "Cost or pricing data" are not required if the proposer proposes an award instrument other than a procurement contract (i.e., cooperative agreement, grant, or other transaction).

Note 2:
Proposers are required to provide the aforementioned cost breakdown as an editable MS Excel spreadsheet, inclusive of calculations formulae, with tabs (material, travel, ODC's) provided as necessary. The Government also requests that the Cost Proposal include MS Excel file(s) that provide traceability between the Bases of Estimate (BOEs) and the proposed costs across all

elements and phases. This includes the calculations and adjustments that are utilized to generate the Summary Costs from the source labor hours, labor costs, material costs, etc. input data. It is requested that the costs and Subcontractor proposals be readily traceable to the Prime Cost Proposal in the provided MS Excel file(s) – although this is not a requirement, providing information in this manner will assist the Government in understanding what is being proposed both technically and in terms of cost realism. NOTE: If the PDF submission differs from the Excel submission, the PDF will take precedence.

Section III. Other Transaction Request, if applicable

All proposers requesting an OT must include a detailed list of payment milestones. Each payment milestone must include the following:

- Milestone description (Do not include proprietary data)
- Completion criteria (Do not include proprietary data)
- Due date
- Dollar Amount (to include, if cost share is proposed, awardee and Government share amounts)

It is noted that, at a minimum, milestones should relate directly to accomplishment of program technical metrics as defined in the BAA and/or the proposer's proposal. See also the "ERI Page 3 Investments" Technology Investment Agreement (TIA) "Model" companion document provided at http://darpa.mil/work-with-us/electronics-resurgence-initiative regarding approaches for pricing payment milestones.

Agreement type, expenditure or fixed-price based, will be subject to negotiation by the Agreements Officer.

Section IV. Other Cost Information

Where the effort consists of multiple portions which could reasonably be partitioned for purposes of funding, these should be identified as options with separate cost estimates.

The cost proposal should include identification of pricing assumptions of which may require incorporation into the resulting award instrument (i.e., use of Government Furnished Property/Facilities/Information, access to Government Subject Matter Experts, etc.).

The proposer should include supporting cost and pricing information in sufficient detail to substantiate the summary cost estimates and should include a description of the method used to estimate costs and supporting documentation.

Cost proposals submitted by FFRDC's (prime or subcontractor) will be forwarded, if selected for negotiation, to their sponsoring organization contracting officer for review to confirm that all required forward pricing rates and factors have been used.

2. Proprietary Information

Proposers are responsible for clearly identifying proprietary information. Submissions containing proprietary information must have the cover page and each page containing such information clearly marked with a label such as "Proprietary" or "Company Proprietary." Note, "Confidential" is a classification marking used to control the dissemination of U.S. Government National Security Information as dictated in Executive Order 13526 and should not be used to identify proprietary business information.

3. Security Information

a. Unclassified Submissions

DARPA anticipates that submissions received under this BAA will be unclassified. No classified proposals will be accepted. However, should a proposer wish to submit classified information, an *unclassified* email must be sent to the BAA mailbox notifying the Technical Office PSO of the submission and the below guidance must be followed.

Security classification guidance and direction via a Security Classification Guide (SCG) and/or DD Form 254, "DoD Contract Security Classification Specification," will not be provided at this time. If a determination is made that the award instrument may result in access to classified information, a SCG and/or DD Form 254 will be issued by DARPA and attached as part of the award.

Classified submissions shall be transmitted in accordance with the following guidance. Additional information on the subjects discussed in this section may be found at http://www.dss.mil/.

If a submission contains Classified National Security Information as defined by Executive Order 13526, the information must be appropriately and conspicuously marked with the proposed classification level and declassification date. Similarly, when the classification of a submission is in question, the submission must be appropriately and conspicuously marked with the proposed classification level and declassification date. Submissions requiring DARPA to make a final classification determination shall be marked as follows:

> "CLASSIFICATION DETERMINATION PENDING. Protect as though classified _____ *(insert the recommended classification level, e.g., Top Secret, Secret or Confidential).*"

NOTE: Classified submissions must indicate the classification level of not only the submitted materials, but also the classification level of the anticipated award.

Proposers submitting classified information must have, or be able to obtain prior to contract award, cognizant security agency approved facilities, information systems, and appropriately cleared/eligible personnel to perform at the classification level proposed. All proposer personnel performing Information Assurance (IA)/Cybersecurity related duties on classified Information

Systems shall meet the requirements set forth in DoD Manual 8570.01-M (Information Assurance Workforce Improvement Program).

When a proposal includes a classified portion, and when able according to security guidelines, we ask that proposers send an e-mail to HR001117S0054@darpa.mil as notification that there is a classified portion to the proposal. When sending the classified portion via mail according to the instructions, proposers should submit six (6) hard copies of the classified portion of their proposal and two (2) CD-ROMs containing the classified portion of the proposal as a single searchable Adobe PDF file. Please ensure that all CDs are well-marked. Each copy of the classified portion must be clearly labeled with HR001117S0054, proposer organization, proposal title (short title recommended), and Copy _ of _.

Proposers choosing to submit classified information from other collateral classified sources (i.e., sources other than DARPA) must ensure (1) they have permission from an authorized individual at the cognizant Government agency (e.g., Contracting Officer, Program Manager); (2) the proposal is marked in accordance with the source Security Classification Guide (SCG) from which the material is derived; and (3) the source SCG is submitted along with the proposal.

Confidential and Secret Information

Use transmission, classification, handling, and marking guidance provided by previously issued SCGs, the DoD Information Security Manual (DoDM 5200.01, Volumes 1 - 4), and the National Industrial Security Program Operating Manual, including the Supplement Revision 1, (DoD 5220.22-M and DoD 5200.22-M Sup. 1) when submitting Confidential and/or Secret classified information.

Confidential and Secret classified information may be submitted via ONE of the two following methods:

- Hand-carried by an appropriately cleared and authorized courier to the DARPA CDR. Prior to traveling, the courier shall contact the DARPA Classified Document Registry (CDR) at 703-526-4052 to coordinate arrival and delivery.

  OR

- Mailed via U.S. Postal Service (USPS) Registered Mail or USPS Express Mail. All classified information will be enclosed in opaque inner and outer covers and double-wrapped. The inner envelope shall be sealed and plainly marked with the assigned classification and addresses of both sender and addressee.

  The inner envelope shall be addressed to:

  Defense Advanced Research Projects Agency
  ATTN: Program Security Officer, MTO
  Reference: HR001117S0054
  675 North Randolph Street

Arlington, VA 22203-2114

The outer envelope shall be sealed with no identification as to the classification of its contents and addressed to:

Defense Advanced Research Projects Agency
Security & Intelligence Directorate, Attn: CDR
675 North Randolph Street
Arlington, VA 22203-2114

Top Secret Information

Use classification, handling, and marking guidance provided by previously issued SCGs, the DoD Information Security Manual (DoDM 5200.01, Volumes 1 - 4), and the National Industrial Security Program Operating Manual, including the Supplement Revision 1, (DoD 5220.22-M and DoD 5200.22-M Sup. 1). Top Secret information must be hand-carried by an appropriately cleared and authorized courier to the DARPA CDR. Prior to traveling, the courier shall contact the DARPA CDR at 703-526-4052 to coordinate arrival and delivery.

Sensitive Compartmented Information (SCI)

SCI must be marked, managed and transmitted in accordance with DoDM 5105.21 Volumes 1 - 3. Questions regarding the transmission of SCI may be sent to the DARPA Technical Office PSO via the BAA mailbox or by contacting the DARPA Special Security Officer (SSO) at 703-812-1970.

Successful proposers may be sponsored by DARPA for access to SCI. Sponsorship must be aligned to an existing DD Form 254 where SCI has been authorized. Questions regarding SCI sponsorship should be directed to the DARPA Personnel Security Office at 703-526-4543.

Special Access Program (SAP) Information

SAP information must be marked in accordance with DoDM 5205.07 Volume 4 and transmitted by specifically approved methods which will be provided by the Technical Office PSO or their staff.

Proposers choosing to submit SAP information from an agency other than DARPA are required to provide the DARPA Technical Office Program Security Officer (PSO) written permission from the source material's cognizant Special Access Program Control Officer (SAPCO) or designated representative. For clarification regarding this process, contact the DARPA Technical Office PSO via the BAA mailbox or the DARPA SAPCO at 703-526-4102.

Additional SAP security requirements regarding facility accreditations, information security, personnel security, physical security, operations security, test security, classified transportation plans, and program protection planning may be specified in the DD Form 254.

NOTE: prior to drafting the submission, if use of SAP Information Systems is to be proposed, proposers must first obtain an Authorization-to-Operate from the DARPA Technical Office PSO (or other applicable DARPA Authorization Official) using the Risk Management Framework (RMF) process outlined in the Joint Special Access Program (SAP) Implementation Guide (JSIG), Revision 3, dated October 9, 2013 (or successor document).

4. Disclosure of Information and Compliance with Safeguarding Covered Defense Information Controls

The following provisions and clause apply to all solicitations and contracts; however, the definition of "controlled technical information" clearly exempts work considered fundamental research and therefore, even though included in the contract, will not apply if the work is fundamental research.

DFARS 252.204-7000, "Disclosure of Information"
DFARS 252.204-7008, "Compliance with Safeguarding Covered Defense Information Controls"
DFARS 252.204-7012, "Safeguarding Covered Defense Information and Cyber Incident Reporting"

The full text of the above solicitation provision and contract clauses can be found at http://www.darpa.mil/work-with-us/additional-baa#NPRPAC.

Compliance with the above requirements includes the mandate for proposers to implement the security requirements specified by National Institute of Standards and Technology (NIST) Special Publication (SP) 800-171, "Protecting Controlled Unclassified Information in Nonfederal Information Systems and Organizations" (see https://doi.org/10.6028/NIST.SP.800-171r1) that are in effect at the time the BAA is issued, or as authorized by the Contracting Officer, not later than December 31, 2017.

For awards where the work is considered fundamental research, the contractor will not have to implement the aforementioned requirements and safeguards; however, should the nature of the work change during performance of the award, work not considered fundamental research will be subject to these requirements.

5. Human Research Subjects/Animal Use

Proposers that anticipate involving Human Research Subjects or Animal Use must comply with the approval procedures detailed at http://www.darpa.mil/work-with-us/additional-baa.

6. Approved Cost Accounting System Documentation

Proposers that do not have a Cost Accounting Standards (CAS) complaint accounting system considered adequate for determining accurate costs that are negotiating a cost- type procurement contract must complete an SF 1408. For more information on CAS compliance, see http://www.dcaa.mil/cas.html. To facilitate this process, proposers should complete the SF 1408 found at http://www.gsa.gov/portal/forms/download/115778 and submit the completed form with the

proposal. To complete the form, check the boxes on the second page, then provide a narrative explanation of your accounting system to supplement the checklist on page one. For more information, see (http://www.dcaa.mil/preaward_accounting_system_adequacy_checklist.html).

7. Section 508 of the Rehabilitation Act (29 U.S.C. § 749d)/FAR 39.2

All electronic and information technology acquired or created through this BAA must satisfy the accessibility requirements of Section 508 of the Rehabilitation Act (29 U.S.C § 794d)/FAR 39.2.

8. Grant Abstract

Per Section 8123 of the Department of Defense Appropriations Act, 2015 (Pub. L. 113-235), all grant awards must be posted on a public website in a searchable format. To comply with this requirement, proposers requesting grant awards must submit a maximum one (1) page abstract that may be publicly posted and explains the program or project to the public. The proposer should sign the bottom of the abstract confirming the information in the abstract is approved for public release. Proposers are advised to provide both a signed PDF copy, as well as an editable (e.g., Microsoft word) copy. Abstracts contained in grant proposals that are not selected for award will not be publicly posted.

9. Small Business Subcontracting Plan

Pursuant to Section 8(d) of the Small Business Act (15 U.S.C. § 637(d)) and FAR 19.702(a)(1), each proposer who submits a contract proposal and includes subcontractors might be required to submit a subcontracting plan with their proposal. The plan format is outlined in FAR 19.704.

10. Intellectual Property

All proposers must provide a good faith representation that the proposer either owns or possesses the appropriate licensing rights to all intellectual property that will be utilized under the proposed effort.

a. For Procurement Contracts

Proposers responding to this BAA requesting procurement contracts will need to complete the certifications at DFARS 252.227-7017. See www.darpa.mil/work-with-us/additional-baa for further information. The Government will use the list during the evaluation process to evaluate the impact of any identified restrictions, and may request additional information from the proposer, as may be necessary, to evaluate the proposer's assertions. If no restrictions are intended, then the proposer should state "NONE." Failure to provide full information may result in a determination that the proposal is not compliant with the BAA – resulting in nonselectability of the proposal.

Technical Data Computer Software To be Furnished With Restrictions	Summary of Intended Use in the Conduct of the Research	Basis for Assertion	Asserted Rights Category	Name of Person Asserting Restrictions
(LIST)	(NARRATIVE)	(LIST)	(LIST)	(LIST)

b. For All Non-Procurement Contracts

Proposers responding to this BAA requesting a Grant, Cooperative Agreement, Technology Investment Agreement, or Other Transaction for Prototype shall follow the applicable rules and regulations governing these various award instruments, but in all cases should appropriately identify any potential restrictions on the Government's use of any Intellectual Property contemplated under those award instruments in question. This includes both Noncommercial Items and Commercial Items. Although not required, proposers may use a format similar to that described in Paragraph 10.a above. The Government may use the list during the evaluation process to evaluate the impact of any identified restrictions, and may request additional information from the proposer, as may be necessary, to evaluate the proposer's assertions. If no restrictions are intended, then the proposer should state "NONE." Failure to provide full information may result in a determination that the proposal is not compliant with the BAA – resulting in nonselectability of the proposal.

11. Patents

Include documentation proving your ownership of or possession of appropriate licensing rights to all patented inventions (or inventions for which a patent application has been filed) that will be utilized under your proposal for the DARPA program. If a patent application has been filed for an invention that your proposal utilizes, but the application has not yet been made publicly available and contains proprietary information, you may provide only the patent number, inventor name(s), assignee names (if any), filing date, filing date of any related provisional application, and a summary of the patent title, together with either: (1) a representation that you own the invention, or (2) proof of possession of appropriate licensing rights in the invention.

12. System for Award Management (SAM) and Universal Identifier Requirements

All proposers must be registered in SAM unless exempt per FAR 4.1102. FAR 52.204-7, "System for Award Management" and FAR 52.204-13, "System for Award Management Maintenance" are incorporated into this BAA. See http://www.darpa.mil/work-with-us/additional-baa for further information.

13. Funding Restrictions

There will be limitations on direct costs such as foreign travel or equipment purchases. Laboratory equipment should include only specialized equipment and tooling specific to the proposed program. Where equipment purchases are proposed, the proposal must include a narrative description for the application requirements.

Preaward costs will not be reimbursed unless a preaward cost agreement is negotiated prior to award.

C. Submission Information

DARPA will acknowledge receipt of all submissions and assign an identifying control number that should be used in all further correspondence regarding the submission. DARPA intends to use electronic mail correspondence regarding HR001117S0054. Submissions may not be submitted by fax or e-mail; any so sent will be disregarded.

Submissions will not be returned. An electronic copy of each submission received will be retained at DARPA and all other non-required copies destroyed. A certification of destruction may be requested, provided the formal request is received by DARPA within 5 days after notification that a proposal was not selected.

All administrative correspondence and questions on this solicitation, including requests for clarifying information on how to submit an abstract or full proposal to this BAA should be directed to HR001117S0054@darpa.mil. DARPA intends to use electronic mail for correspondence regarding HR001117S0054. Proposals and abstracts may not be submitted by fax or e-mail; any so sent will be disregarded. DARPA encourages use of the Internet for retrieving the BAA and any other related information that may subsequently be provided.

1. Submission Dates and Times

a. Full Proposal Date

The full proposal must be submitted via the DARPA BAA website on or before 1:00 PM, Eastern Time, November 14, 2017. If deemed compliant, the Government will evaluate all such proposals in the initial round of selections.

Additionally, proposals may be submitted after the above due date until 1:00 PM, Eastern Time, January 31, 2018 which, if deemed compliant, will be reviewed at the Government's discretion, depending upon the availability of funding.

Proposers are warned that the likelihood of available funding is greatly reduced for proposals submitted after the initial closing date deadline.

b. Frequently Asked Questions (FAQ)

DARPA will post a consolidated Question and Answer (FAQ) document on a regular basis. To access the posting go to: http://www.darpa.mil/work-with-us/opportunities. Under the HR001117S0054 summary will be a link to the FAQ. Submit your question/s by e-mail to HR001117S0054@darpa.mil. In order to receive a response sufficiently in advance of the proposal due date, send your question/s on or before 1:00 PM, Eastern Time, November 1st , 2017.

2. Proposal Submission Information

The typical proposal should express a consolidated effort in support of one or more related technical concepts or ideas. Disjointed efforts should not be included into a single proposal. Proposals not meeting the format described in the BAA may not be reviewed.

a. For Proposers Requesting Grants or Cooperative Agreements:

Proposers requesting grants or cooperative agreements may submit proposals through one of the following methods: (1) hard copy mailed directly to DARPA; or (2) electronic upload per the instructions at http://www.grants.gov/applicants/apply-for-grants.html. Grant or cooperative agreement proposals may not be submitted through any other means. If proposers intend to use Grants.gov as their means of submission, then they must submit their entire proposal through Grants.gov; applications cannot be submitted in part to Grants.gov and in part as a hard-copy. Proposers using the Grants.gov do not submit paper proposals in addition to the Grants.gov electronic submission.
Grants.gov requires proposers to complete a one-time registration process before a proposal can be electronically submitted. If proposers have not previously registered, this process can take between three business days and four weeks. For more information about registering for Grants.gov, see www.darpa.mil/work-with-us/additional-baa. See the Grants.gov registration checklist at http://www.grants.gov/web/grants/register.html for registration requirements and instructions.

Once Grants.gov has received a proposal submission, Grants.gov will send two email messages to advise proposers as to whether or not their proposals have been validated or rejected by the system; IT MAY TAKE UP TO TWO DAYS TO RECEIVE THESE EMAILS. The first email will confirm receipt of the proposal by the Grants.gov system; this email only confirms receipt, not acceptance, of the proposal. The second will indicate that the application has been successfully validated by the system prior to transmission to the grantor agency or has been rejected due to errors. If the proposal is validated, then the proposer has successfully submitted their proposal. If the proposal is rejected, the proposed must be corrected and resubmitted before DARPA can retrieve it. If the solicitation is no longer open, the rejected proposal cannot be resubmitted. Once the proposal is retrieved by DARPA, the proposer will receive a third email from Grants.gov. To avoid missing deadlines, proposers should submit their proposals in advance of the final proposal due date with sufficient time to receive confirmations and correct any errors in the submission process through Grants.gov. For more information on submitting proposals to Grants.gov, visit the Grants.gov submissions page at:
http://www.grants.gov/web/grants/applicants/apply-for-grants.html.

Proposers electing to submit grant or cooperative agreement proposals as hard copies must complete the SF 424 R&R form (Application for Federal Assistance, Research and Related) available on the Grants.gov website
http://apply07.grants.gov/apply/forms/sample/RR_SF424_2_0-V2.0.pdf. Technical support for Grants.gov submissions may be reached at 1-800-518-4726 or support@grants.gov.

b. For Proposers Requesting Contracts or Other Transaction Agreements

Proposers requesting contracts or other transaction agreements must submit proposals via DARPA's BAA Website (https://baa.darpa.mil). Note: If an account has already been created for the DARPA BAA Website, this account may be reused. If no account currently exists for the DARPA BAA Website, visit the website to complete the two-step registration process. Submitters will need to register for an Extranet account (via the form at the URL listed above) and wait for two separate e-mails containing a username and temporary password. After accessing the Extranet, submitters may then create an account for the DARPA BAA website (via the "Register your Organization" link along the left side of the homepage), view submission instructions, and upload/finalize the proposal. Proposers using the DARPA BAA Website may encounter heavy traffic on the submission deadline date; it is highly advised that submission process be started as early as possible.

All unclassified full proposals submitted electronically through the DARPA BAA website must be uploaded as zip files (.zip or .zipx extension). The final zip file should not exceed 50 MB in size. Only one zip file will be accepted per submission and submissions not uploaded as zip files will be rejected by DARPA.

NOTE: YOU MUST CLICK THE 'FINALIZE FULL PROPOSAL' BUTTON AT THE BOTTOM OF THE CREATE FULL PROPOSAL PAGE. FAILURE TO DO SO WILL RESULT IN YOUR PROPOSAL NOT BEING OFFICIALLY SUBMITTED TO THIS BAA AND THEREFORE NOT BEING REVIEWED.

Classified submissions and proposals requesting assistance instruments (grants or cooperative agreements) should NOT be submitted through DARPA's BAA Website (https://baa.darpa.mil), though proposers will likely still need to visit https://baa.darpa.mil to register their organization (or verify an existing registration) to ensure the BAA office can verify and finalize their submission.

Please note that the DoD-issued certificate associated with the BAA website is not recognized by all commercial certificate authorities, resulting in untrusted connection errors/messages. You can either bypass the warning (possibly by adding https://baa.darpa.mil to your listed of trusted sites, or darpa.mil as a trusted domain), or visit DISA's site to download the Root Certificate Authority (CA): http://dodpki.c3pki.chamb.disa.mil/rootca.html.

Technical support for DARPA's BAA Website may be reached at BAAT_Support@darpa.mil, and is typically available during regular business hours (9:00 AM - 5:00 PM EST, Monday - Friday).

c. Classified Submission Information

See Section IV.B.4, "Security Information," for guidance on submitting classified abstracts and proposals.

V. Application Review Information

A. Evaluation Criteria

1. Overall Scientific and Technical Merit

The proposed technical approach is innovative, feasible, achievable, and complete.

The proposal should be supported by a technical team with the expertise and experience to accomplish the proposed task. The proposer's prior experience in similar efforts should clearly demonstrate an ability to deliver products that meet the proposed technical performance. A clear and feasible plan for delivery of high quality software with open interfaces is provided.

Task descriptions and associated technical elements provided are complete and in a logical sequence with all proposed deliverables clearly defined such that a final outcome that achieves the goal can be expected as a result of award. The proposal identifies major technical risks and planned mitigation efforts are clearly defined and feasible.

2. Potential Contribution and Relevance to the DARPA Mission of Supporting National Security

The potential contributions of the proposed effort are relevant to the national technology base. Specifically, DARPA's mission is to make pivotal early technology investments that create or prevent strategic surprise for U.S. National Security.

Proposals should demonstrate rapid physical design of Systems-on-Chip and how such systems can enable new technologies or circuits to be incorporated into DoD systems in record time.

The proposed transition plan clearly demonstrates a comprehensive understanding of competing technical approaches on the market and in the lab today, the new capabilities that this technology would provide, and how this new technology is expected to compare on not only a performance basis but also a cost basis. The proposed transition plan demonstrates what impact the implementation of this technology could have on national defense and how this technology would be matured and transitioned to commercial and DoD users.

3. Impact on the Overall Electronics Landscape

The proposed research is appropriate for pre-competitive, basic or applied DoD research funding. The technology represents a radical departure from current trends in the electronics industry – such as the diminishing access, rising costs, and growing complexities of leading edge circuit design – and has the potential to broadly impact the semiconductor industry in the 2025 to 2030 timeframe.

4. Cost Realism

The proposed costs are realistic for the technical and management approach and accurately reflect the technical goals and objectives of the solicitation. The proposed costs are consistent

with the proposer's Statement of Work and reflect a sufficient understanding of the costs and level of effort needed to successfully accomplish the proposed technical approach. The costs for the prime proposer and proposed subawardees are substantiated by the details provided in the proposal (e.g., the type and number of labor hours proposed per task, the types and quantities of materials, equipment and fabrication costs, travel and any other applicable costs and the basis for the estimates).

Specifically for these programs, for which simultaneous impacts to the commercial sector and DoD are expected, the level of performer cost share will be considered as a significant element of the Cost Realism evaluation. DARPA recognizes that undue emphasis on cost may motivate proposers to offer low-risk ideas with minimum uncertainty and to staff the effort with junior personnel in order to be in a more competitive posture. DARPA discourages such cost strategies. It is expected that the effort will leverage all available relevant prior research in order to obtain the maximum benefit from the available funding.

B. Review and Selection Process

1. Review Process

It is the policy of DARPA to ensure impartial, equitable, comprehensive proposal evaluations based on the evaluation criteria listed in Section V.A, and to select the source (or sources) whose offer meets the Government's technical, policy, and programmatic goals.

DARPA will conduct a scientific/technical review of each conforming proposal. Conforming proposals comply with all requirements detailed in this BAA; proposals that fail to do so may be deemed non-conforming and may be removed from consideration. Proposals will not be evaluated against each other since they are not submitted in accordance with a common work statement. DARPA's intent is to review proposals as soon as possible after they arrive; however, proposals may be reviewed periodically for administrative reasons.

Award(s) will be made to proposers whose proposals are determined to be the most advantageous to the Government, all factors considered, including the potential contributions of the proposed work to the overall research program and the availability of funding for the effort.

It is the policy of DARPA to ensure impartial, equitable, comprehensive proposal evaluations based on the evaluation criteria listed above and to select the source (or sources) whose offer meets the Government's technical, policy, and programmatic goals. Pursuant to FAR 35.016, the primary basis for selecting proposals for acceptance shall be technical, importance to agency programs, and fund availability. In order to provide the desired evaluation, qualified Government personnel will conduct reviews and (if necessary) convene panels of experts in the appropriate areas.

2. Handling of Source Selection Information

DARPA policy is to treat all submissions as source selection information (see FAR 2.101 and 3.104), and to disclose their contents only for the purpose of evaluation. Restrictive notices

notwithstanding, during the evaluation process, submissions may be handled by support contractors for administrative purposes and/or to assist with technical evaluation. All DARPA support contractors performing this role are expressly prohibited from performing DARPA-sponsored technical research and are bound by appropriate nondisclosure agreements.

Subject to the restrictions set forth in FAR 37.203(d), input on technical aspects of the proposals may be solicited by DARPA from non-Government consultants/experts who are strictly bound by the appropriate non-disclosure requirements.

3. Federal Awardee Performance and Integrity Information (FAPIIS)

Per 41 U.S.C. 2313, as implemented by FAR 9.103 and 2 CFR § 200.205, prior to making an award above the simplified acquisition threshold, DARPA is required to review and consider any information available through the designated integrity and performance system (currently FAPIIS). Awardees have the opportunity to comment on any information about themselves entered in the database, and DARPA will consider any comments, along with other information in FAPIIS or other systems prior to making an award.

VI. Award Administration Information

A. Selection Notices

1. Proposals

As soon as the evaluation of a proposal is complete, the proposer will be notified that (1) the proposal has been selected for funding pending contract negotiations, in whole or in part, or (2) the proposal has not been selected. These official notifications will be sent via email to the Technical POC identified on the proposal coversheet.

B. Administrative and National Policy Requirements

1. Meeting and Travel Requirements

All key participants are required to attend the program kickoff meeting. Performers should also anticipate regular program-wide PI Meetings and periodic site visits at the Program Manager's discretion. Performers will be required to attend and participate in bi-annual week long software integration exercises.

2. FAR and DFARS Clauses

Solicitation clauses in the FAR and DFARS relevant to procurement contracts and FAR and DFARS clauses that may be included in any resultant procurement contracts are incorporated herein and can be found at www.darpa.mil/work-with-us/additional-baa.

3. Controlled Unclassified Information (CUI) on Non-DoD Information Systems

Further information on Controlled Unclassified Information on Non-DoD Information Systems is incorporated herein can be found at www.darpa.mil/work-with-us/additional-baa.

4. Representations and Certifications

If a procurement contract is contemplated, prospective awardees will need to be registered in the SAM database prior to award and complete electronic annual representations and certifications consistent with FAR guidance at 4.1102 and 4.1201; the representations and certifications can be found at www.sam.gov. Supplementary representations and certifications can be found at http://www.darpa.mil/work-with-us/additional-baa.
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5. Terms and Conditions

A link to the DoD General Research Terms and Conditions for Grants and Cooperative Agreements and supplemental agency terms and conditions can be found at http://www.darpa.mil/work-with-us/contract-management#GrantsCooperativeAgreements.

C. Reporting

The number and types of reports will be specified in the award document, but will include as a minimum quarterly technical and monthly financial status reports. The reports shall be prepared and submitted in accordance with the procedures contained in the award document and mutually agreed on before award. Reports and briefing material will also be required as appropriate to document progress in accomplishing program metrics. A Final Report that summarizes the project and tasks will be required at the conclusion of the performance period for the award, notwithstanding the fact that the research may be continued under a follow-on vehicle.

D. Electronic Systems

1. Wide Area Work Flow (WAWF)

Unless using another means of invoicing, performers will be required to submit invoices for payment directly via to https://wawf.eb.mil. Registration in WAWF will be required prior to any award under this BAA.

2. i-Edison

The award document for each proposal selected for funding will contain a mandatory requirement for patent reports and notifications to be submitted electronically through i-Edison (https://public.era.nih.gov/iedison).

3. Contract Execution Reporting Service (CERS)

The award document for each proposal selected for funding will contain a mandatory requirement for technical and status reports to be submitted electronically through DARPA's CERS (or similar) web-based tool.

VII. Agency Contacts

Administrative, technical or contractual questions should be sent via e-mail to HR001117S0054@darpa.mil. All requests must include the name, email address, and phone number of a point of contact.

The technical POC for this effort is:
Mr. Andreas Olofsson
DARPA/MTO
ATTN: HR001117S0054
675 North Randolph Street
Arlington, VA 22203-2114

VIII. Other Information

A. Proposers Day

The combined Page 3 Design Proposers Day will be held on September 22nd, 2017 in Mountain View, CA. Advance registration is required for the physical meeting. See DARPA-SN-17-75 posted at www.fbo.gov for details on all Page 3 Proposers Days. Attendance at the Page 3 Design Proposers Day is not required to propose to this solicitation.

B. Protesting

For information concerning agency level protests see http://www.darpa.mil/work-with-us/additional-baa#NPRPAC.